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GRADO EN INGENIERÍA EN TÉCNOLOGÍAS INDUSTRIALES

DEGREE FINAL THESIS

A PRACTICAL APPROACH TO TESTING 18650 LI-ION CELLS AND DEVELOPING STATE OF CHARGE AND THERMAL MODELS

Author: Daniel Aguilera Irala

Supervisor: Pablo Ayala Santamaría

Ann Arbor, USA and Madrid, Spain, July 2025

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A practical approach to testing 18650 Li-Ion cells and developing state-of-charge and thermal models

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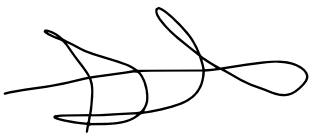
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I would like to express my sincere gratitude to Pablo Ayala Santamaría, my project supervisor, without whose help and support this work would not have been possible. Through the research scholarship at ICAI, I have not only learned about batteries but also how to tackle complex engineering challenges, build and test prototypes, and parameterize and scale models. Thanks to this positive experience and the support I received, I decided to continue and deepen my studies in this field, which became the focus of this project. I also want to thank the entire ISC Formula Student Racing team family, whose support helped me build prototypes and gave me my first opportunity to work with real-world batteries and develop electrical systems. There are many people to thank, but I am especially grateful to Javier Rodríguez Criado, Raúl Guerra Morán, Miguel Medina Lazcano, Javier Rodríguez Juliani, and Ignacio Núñez Gómez. Finally, I want to thank ICAI for the excellent academic and personal education I received throughout my degree, which enabled me to successfully complete this work.

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Collaborating Entity: ICAI – Universidad Pontificia Comillas

ABSTRACT

In a world increasingly powered by renewable energy, lithium-ion batteries play a pivotal role in modern energy storage systems and electric mobility solutions. However, their performance and safety depend heavily on accurate characterization of their electrochemical and thermal dynamics. This study presents a comprehensive and practical approach to testing 18650 Li-ion cells (Sony-Murata VTC6) using the Galvanostatic Intermittent Titration Technique (GITT) to extract open-circuit voltage (OCV), ohmic resistance (R1), polarization resistance (R2), and capacitance (C) as functions of state of charge (SOC) across multiple C-rates (0.5C, 1C, 2C, 3C).

Custom hardware test benches were developed in-house for both single-cell and six-cell parallel configurations, featuring Arduino-based control, variable resistor loads, and an array of temperature sensors. The extracted parameters were scaled between single-cell and parallel configurations to study how cell electrochemical behavior scales when assembled in parallel. Comparative analysis showed that SOC-OCV profile scaled predictably from single cell to parallel configuration, while internal impedance and capacitance displayed greater variability. The ECM parameters were incorporated into a MATLAB Simscape cell model, which was then scaled to parallel, module, and pack levels, and used to run real-world simulation load curves and standardized drive cycles. Additionally, destructive external short-circuit tests were carried out to quantify thermal-runaway risk at cell level. The methodology proposed provides a low-cost and scalable framework for cell characterization, suitable for academic and small-scale laboratories.

Key Words: Lithium-ion cell characterization, battery cyclers, battery safety, GITT, battery parallel, ECM, SOC, OCV, internal cell impedance, fire safety, model scalability

1. Introduction

The global transition to sustainable energy hinges on efficient energy storage solutions, with lithium-ion batteries leading the way thanks to their high energy density, long cycle life, and rapid charge–discharge capabilities. As renewables like wind and solar continue to grow, reaching 510 GW of installed capacity worldwide [1], the need for reliable, high-performance energy storage systems becomes more urgent than ever before. Lithium-ion batteries are not only central to grid-scale storage but also power everything from electric vehicles (EVs) and hybrids to buses, scooters, and personal electronics. Their ubiquity in modern energy systems makes optimizing their performance and improving their safety, a critical engineering challenge.

However, the dynamic behavior and safety of lithium-ion cells depend heavily on electrochemical parameters, such as open-circuit voltage (OCV), internal resistance (R1, R2), and capacitance (C), that vary nonlinearly with state of charge (SOC), temperature, and aging. Accurate characterization of these parameters under realistic load conditions is essential for developing robust battery management systems (BMS), extending battery life, and reducing failure risks. To obtain the parameters for the equivalent cell models, battery cells are often cycled (tested) by the manufacturers using commercial battery cyclers, but these tend to cost in order of $25,000 [2]. This presents a significant barrier for academic labs and small-scale developers.

To address this, this study introduces a low-cost, practical methodology for testing both single-cell and parallel-cell configurations using custom-built test benches based on microcontrollers and discrete load banks. In addition to closing the cost-accessibility gap, this thesis tackles a second major limitation in current battery research: the lack of testing and modeling at parallel, module, and pack levels. Most available data is limited to single-cell tests, typically provided by manufacturers. This work develops and validates a scalable modeling framework, based on scaled Equivalent Circuit Models (ECM) and SOC estimations, that extends single cell parameters to larger assemblies.

2. State of the art

To accurately simulate the electrical behavior of lithium-ion batteries, Equivalent Circuit Models (ECMs) are commonly employed. These models represent the battery using combinations of internal impedances and capacitors that emulate the batteries dynamic response during charge and discharge. Among several ECM configurations analyzed in the literature, the first-order Thevenin model (see Figure 1) has proven to be a good trade-off between complexity and accuracy [3]. The internal impedance R1, represents the immediate ohmic drop experienced when exposed to a load, whilst the R2 and C are used to represent the polarization effects and cell transient dynamics.

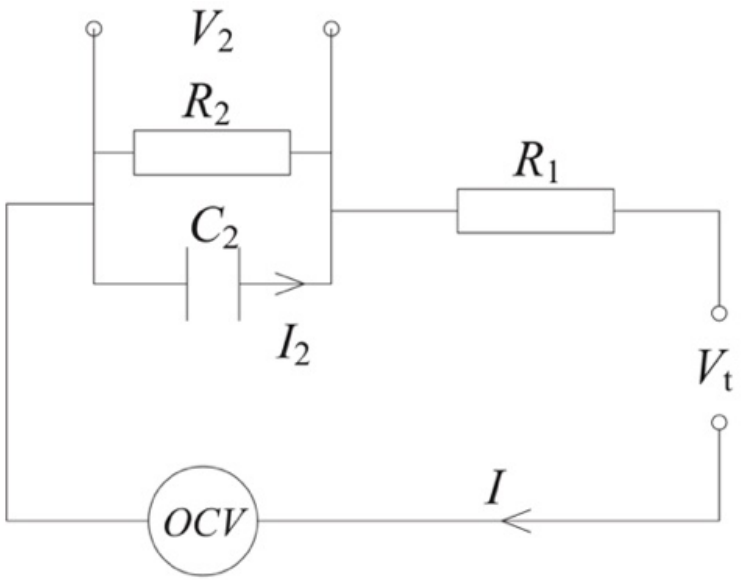


Figure 1: First order Thevenin Equivalent Circuit Model [3]

To extract these parameters as a function of State of Charge (SOC), the cells are discharged following the Galvanostatic Intermittent Titration Technique (GITT) proposed by Liu et al. [3]. As shown in Figure 2, GITT involves discharging the battery in constant current pulses (in this case 18A) followed by disconnection periods. During these rest phases, the terminal voltage decays exponentially toward the Open Circuit Voltage (OCV), allowing each component of the ECM to be fitted from the response:

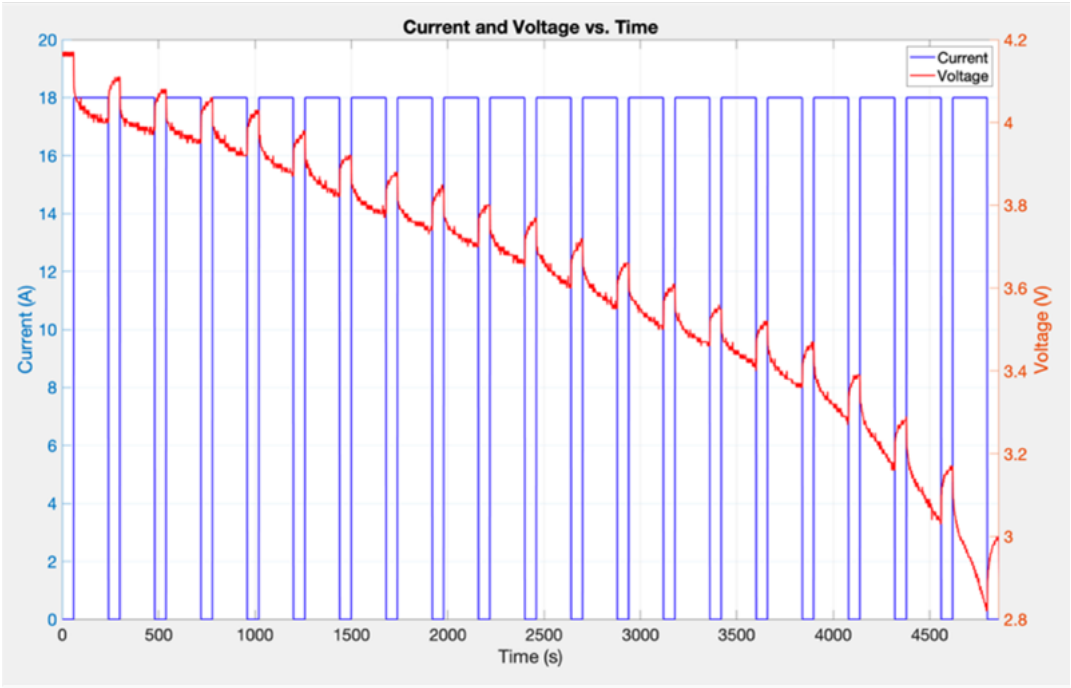


Figure 2: Current and Voltage vs Time for GITT cycle at 1C [3]

$$R1\ (SOC) = \frac{V_0(0+) - V_0(0-)}{I}$$

OCV, R2, C2 are calculated using an exponential fit of the voltage from $V_0(0+)$ to V_1, which is the voltage 60s after the disconnect:

$$v(t) = a * e^{-bt} + c$$

$$OCV\ (SOC) = c$$

$$R2(SOC) = a/I$$

$$C2(SOC) = 1/(R2 * b)$$

Figure 3 shows a close-up of two disconnection periods, showing the instantaneous voltage jump (captured by R_1) and the transient settling behavior (modeled by R_2 and C).

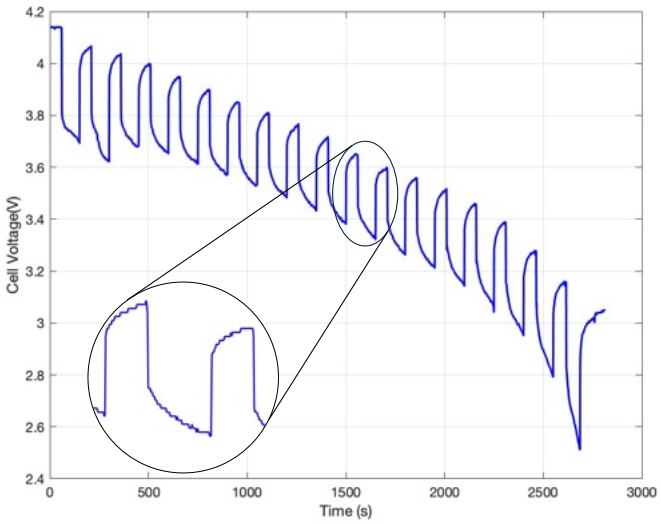


Figure 3: Close-up of GITT constant 1C current pulses and voltage vs time

These GITT pulses are repeated every 5% of State of Charge (SOC), resulting in 20 steps from full to empty discharge [4]. Before continuing with the description of the experimental setup for the test banks, it is important to clarify the concept of SOC. State of Charge defined as the ratio of remaining capacity to nominal capacity. SOC is not directly measurable and must be estimated. One common approach is Coulomb Counting, which integrates the current over time. While straightforward, this method is prone to cumulative errors due to sensor drift and uncertainty in the initial SOC value [5]. Alternatively, model-based methods such as the Kalman Filter offer a more accurate solution [6]. By combining real-time current and voltage measurements with an Equivalent Circuit Model (ECM), the Kalman Filter continuously updates the SOC estimate and reduces drift, making it especially effective under dynamic load conditions.

3. Experiment Description

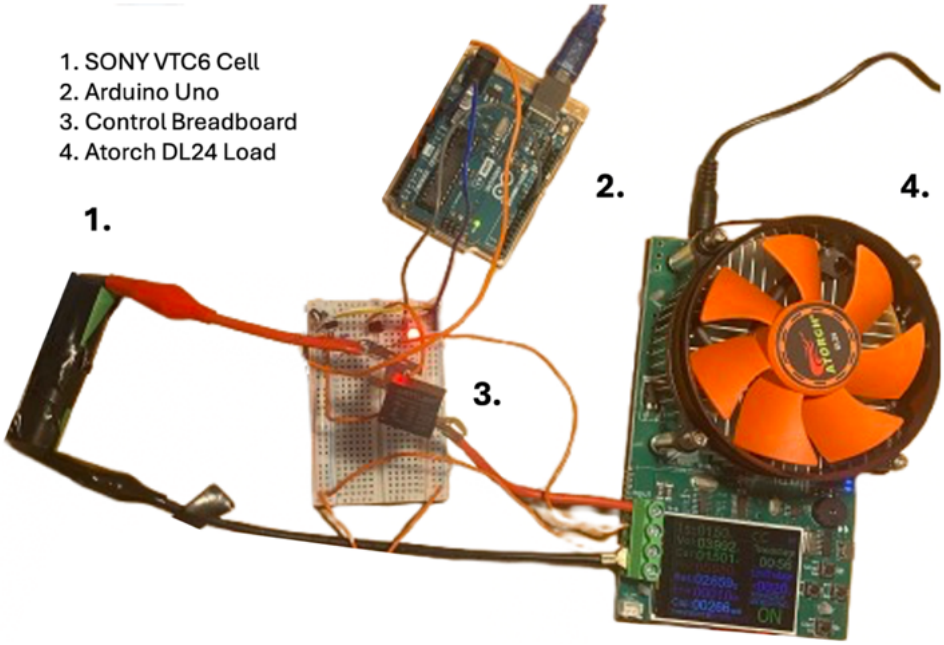


Figure 4: Single cell battery test bank setup

Figure 4 shows the single-cell battery test bank setup, which uses an Arduino Uno as the central controller and an Atorch DL24 as the programmable load. The Arduino manages the discharge cycles, monitors cell voltage and current, and enforces safety cutoffs. The discharge GITT profile is implemented by toggling a power relay. The test bench supports discharge currents up to 20 A with a maximum regulation error of ±0.01 A, delivering up to 180 W of power, sufficient for testing a single 18650 cell up to 6C.

In addition to the single-cell test bench, a higher-power custom test bank was developed to support six-cell parallel configurations, as shown in Figure 5. The system consists of three main components: a variable resistance load, a battery holder with copper busbars, and an Arduino MEGA 2560, which acts as both the system controller and data logger. To handle the significantly higher current demand, up to 54 A, corresponding to a 3C discharge rate for six Sony VTC6 cells, all conductive pathways were redesigned for the upgraded high-current requirements. Several improvements were introduced over the single-cell setup. The parallel test bank supports multi-point thermal monitoring, with sensors positioned at the top, middle, and bottom of each cell, as well as on the load resistors and in the ambient environment. The previous power relay was replaced with a TE Kilovac series contactor, rated for high-current switching, to ensure reliable operation during repeated discharge pulses. Unlike the single-cell setup, which used an array of MOSFETs the parallel test bank employs a discrete variable impedance load, consisting of 17 resistors and 11 relays. Six of these are large ceramic resistors that carry

the bulk of the current and remain permanently engaged during testing. The remaining resistors are selectively activated via relays to adjust the total resistance in real time to regulate the current as the cell discharges.

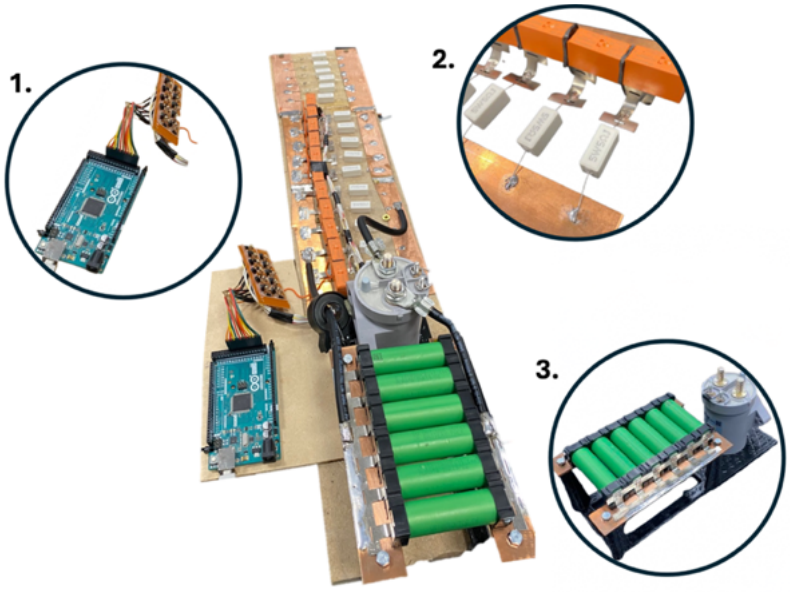


Figure 5: 6 cell parallel battery test bank setup

This thesis focuses on a single cell type: the SONY-MURATA US18650VTC6 (3000 mAh). The VTC6 was selected due to its widespread use, availability of comparable test data, and relatively low cost, which aligns with the overall project budget. The cells were tested at 0.5C, 1C, 2C, and 3C, both at the single-cell and parallel configurations, with three trials conducted per discharge rate at each scale.

4. Battery Cycling Results

After completing all the discharge cycles, the OCV, R1, R2, and C values were calculated for each disconnection. Figure 6a shows the average OCV–SOC profile under GITT for a single cell at different C-rates. It can be observed that, at a given SOC, the OCV decreases as the discharge C-rate increases. Quantitatively, the OCV at 3C is approximately 0.15 V lower than at 0.5C in the mid-SOC range, directly reducing the extractable energy—both in the single-cell and parallel configurations at 2C and 3C. Additionally, all C-rates exhibit a steeper voltage drop below 40% SOC. This knee suggests a shift in dominant reaction kinetics or the onset of mass-transport limitations as the electrode nears the end-of-discharge region. The convergence of the OCV curves at low SOC may indicate that C-rate effects become negligible once the electrode materials are nearly depleted.

a) b)

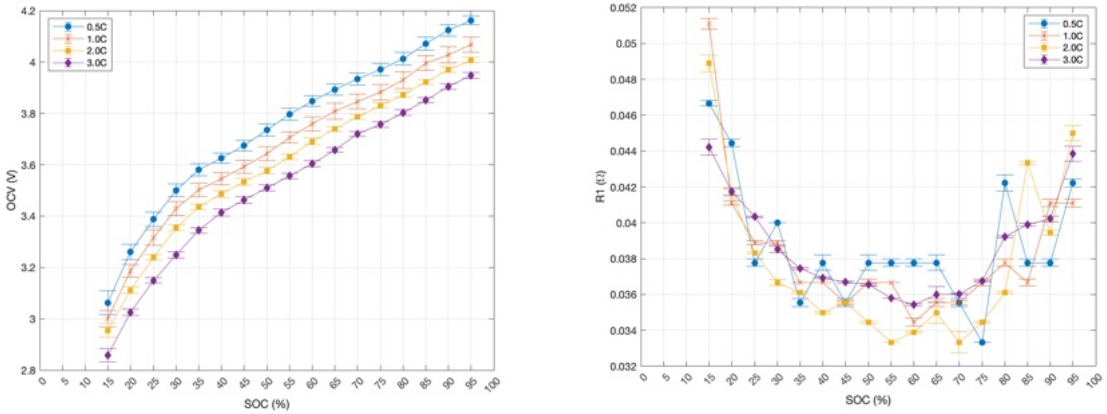


Figure 6 a,b: C-rate dependence of the dynamic behavior of a single cell under GITT cycling: a) OCV(V) vs SOC (%), b) R1 (Ω) vs SOC (%)

For the single cell, internal resistance (R1) follows a U-shaped trend, with the highest values at the start (>95% SOC) and end (<20% SOC) of the discharge, and a clear minimum around 40–60% SOC (Figure 6b). This behavior is expected: at high SOC, lithium ions are tightly packed in the anode, making it harder for them to leave, while at low SOC, a similar phenomenon happens in the tightly packed cathode.

Figure 7 provides more insight into how ECM parameters scale when connected in parallel. In Figure 7a, all C-rate OCV–SOC curves show a similar slope (~0.01 V/% SOC) during early discharge, with 2C and 3C offset downward by about 0.05 V and 0.1 V, respectively. Below 40% SOC, the voltage drops more steeply, and all curves converge between 2.85 V and 2.95 V near 15% SOC. For R1, the parallel configuration shows much lower average values (0.006–0.002 Ω), but more noise and oscillations above 30% SOC, likely due to more significant voltage measurement resolution limitations.

a) b)

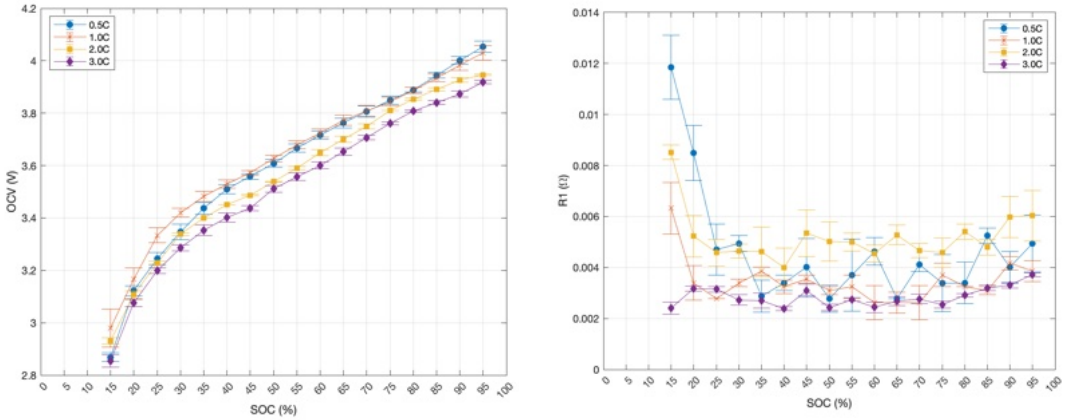


Figure 7 a,b: C-rate dependence of the dynamic behavior of a 6 cell parallel under GITT cycling: a) OCV(V) vs SOC (%), b) R1 (Ω) vs SOC (%)

After processing the single-cell and parallel ECM results, a comparative analysis was conducted to evaluate how well the models scaled. The SOC–OCV profile scaled predictably from the single-cell to the parallel configuration; however, internal impedance and capacitance showed greater variability. For example, the internal impedance in the parallel configuration was 17 times lower than in the single-cell case, far from the expected 6× reduction based on cell count. Meanwhile, the capacitance of the scaled-down parallel model was 100 to 1000 times larger than expected. These discrepancies highlight both the complexity of scaling transient behavior and the limitations imposed by low-resolution voltage measurements. The use of a 10-bit Arduino ADC, with a quantization error of ±4.9 mV, limited the ability to accurately capture the transient voltage response (~50 mV) used to extract dynamic parameters such as R2 and C. Another challenge was analyzing R2 and C independently. Benchmarking the time constant directly would have been a simpler and more robust approach, as both R2 and C were highly sensitive to their relative weights during exponential fitting and, as a result, were not directly comparable after scaling.

5. Battery modelling and scaling

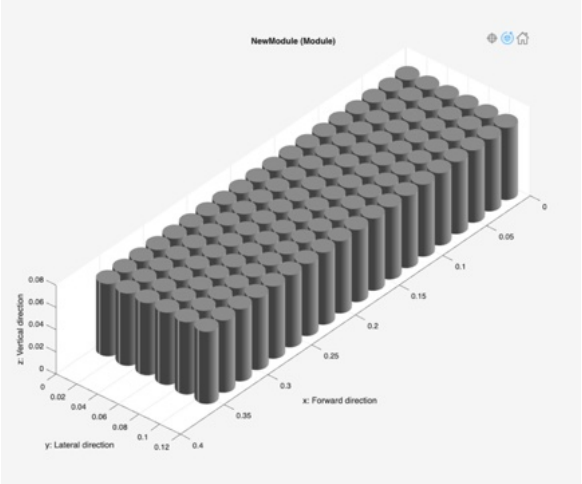


Figure 8: IFS-06 Formula Student Car battery module Simscape assembly

Using the single-cell ECM's parameters, a MATLAB Simscape model was built, which was scaled to parallel, module (as seen in Figure 8) and pack size. Subsequently, the pack was stress-tested under discharge rates of 0.5C, 1C, 2C, and 3C to compare terminal voltage profiles, heat generation, and SOC trends. To replicate real-world EV usage, the full pack model was also run through the FTP-75 urban driving cycle, taken from Simscape's standardized drive cycle library. This test introduced stop-and-go load behavior and provided a more realistic view of how the pack responds under city driving. For simplification, regenerative braking was excluded. Figure 9 shows the current and terminal for the EV battery pack across the FTP-75 drive cycle.

a) b)

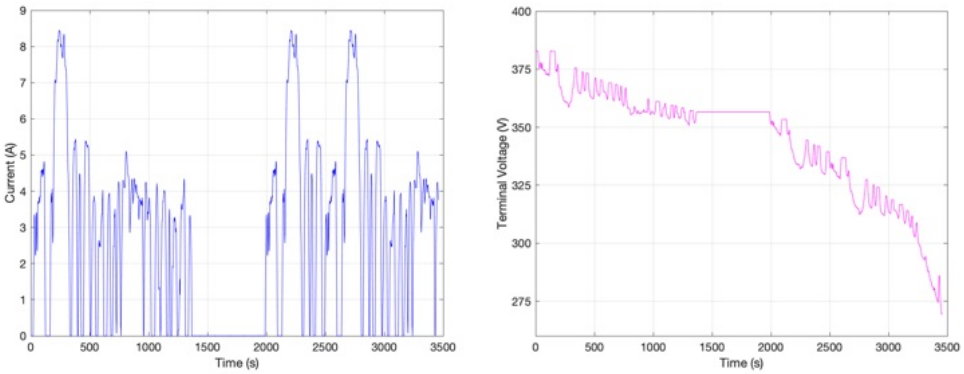


Figure 9: IFS-06 Formula Student Race Car Battery Pack FTP-75 Drive Cycle Simulation: a) Battery Current (A) vs Time (s), b) Terminal Voltage (V) vs Time (s)

6. Thermal Runaway

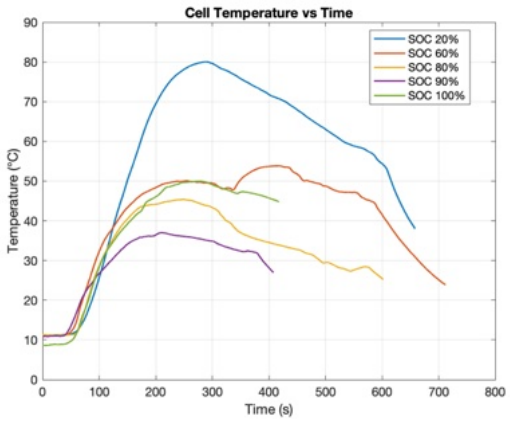


Figure 10: VTC6 Cell Temperature (Celsius) vs Time (s) after External Short-Circuit

After completing all battery cycling experiments, a series of destructive short-circuit tests were conducted to study the thermal runaway behavior of Sony-Murata VTC6 18650 cells. The goal was to assess how State of Charge (SOC) affects both the likelihood and severity of thermal runaway. Five cells were tested at different SOC levels 20%, 60%, 80%, 90%, and 100%, using the external short-circuit Interestingly, none of the cells reached full thermal runaway, even at 100% SOC. The highest temperature recorded was 80 °C in the 20% SOC cell, which notably did not vent, possibly because its safety tab remained intact, allowing internal heat and pressure to accumulate. In contrast, all higher-SOC cells showed clear venting behavior, which likely relieved internal pressure and prevented further temperature rise. The venting events seem to have acted as a safety mechanism, avoiding runaway. Additionally, it is important to note that the tests were conducted outdoors at 10 °C, which most likely significantly slowed the rapid temperature increase.

7. Conclusion

This study presented a cost-effective, practical approach to battery characterization by developing two custom test benches for single cells and six-cell parallel banks. Both setups performed GITT discharges up to 3C, with two current regulation methods explored: a precise MOSFET-based variable resistor and a relay-controlled shunt resistor array for higher currents.

Key electrochemical parameters (OCV, R1, R2, C) were extracted across multiple C-rates, creating equivalent circuit models for single and parallel cells. While OCV–SOC profiles scaled predictably between single and parallel configurations, impedance and capacitance showed more variability. Using the single-cell data, an ECM database was created and integrated into MATLAB Simscape for fast, scalable simulations validated with FTP-75 drive cycle in a 95S6P battery pack from a Formula Student vehicle.

Destructive short-circuit tests showed no thermal runaway; cells that vented limited temperature rise, whereas the 20% SOC cell heated the most due to lack of venting. Secondary thermal events suggest complex internal dynamics during failure. Overall, this work offers a comprehensive and accessible method for characterizing 18650 Li-ion cells and scaling ECMs, providing valuable tools and insights for future academic and small-scale industrial researchers.

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PROPUESTA METODOLÓGICA PARA LA CARACTERIZACIÓN DE CELDAS DE ION-LITIO 18650 Y EL DESARROLLO DE MODELOS DE ESTADO DE CARGA Y TÉRMICOS.

Autor: Aguilera Irala, Daniel.
Director: Ayala Santamaría, Pablo.

Entidad Colaboradora: ICAI – Universidad Pontificia Comillas

RESUMEN DEL PROYECTO

En un mundo cada vez más impulsado por energías renovables, las baterías de ion-litio desempeñan un papel esencial en el almacenamiento de energía y la movilidad eléctrica. No obstante, su rendimiento y seguridad dependen de una caracterización precisa de su comportamiento electroquímico y térmico. Este estudio presenta un enfoque práctico para probar celdas 18650 (Sony-Murata VTC6) mediante la Técnica de Valoración Galvanostática Intermitente (GITT), con el objetivo de extraer parámetros como la tensión en circuito abierto (OCV), la resistencia óhmica (R1), la resistencia de polarización (R2) y la capacitancia (C) en función del estado de carga (SOC) y bajo distintas tasas C (0,5C, 1C, 2C y 3C).

Se diseñaron dos bancadas de prueba: una para probar celdas individualmente y para paralelos de seis celdas, utilizando placas Arduino, resistencias variables y sensores de temperatura digitales. Se compararon los parámetros obtenidos en ambos casos para analizar cómo escalaban las dinámicas electroquímicas al conectar las celdas en paralelo. El perfil SOC-OCV mostró una escalabilidad predecible, mientras que la impedancia y la capacitancia interna presentaron mayor variabilidad. Los parámetros extraídos se implementaron en MATLAB Simscape para construir un modelo de circuito equivalente, que fue escalado de una celda a un paralelo, módulo y acumulador. El modelo permitió simular distintos ciclos de conducción, observando su respuesta frente a curvas de carga reales. Finalmente, se realizaron ensayos destructivos de cortocircuito externo para cuantificar el riesgo de *thermal runaway* (embalamiento térmico) a nivel de celda. La metodología propuesta ofrece una solución económica y fácilmente replicable, ideal para laboratorios académicos y de pequeña escala que busquen caracterizar celdas de forma práctica, rigurosa y eficiente.

Palabras clave: Modelado baterías ion-litio, cicladores de baterías, bancada, GITT, ECM, SOC

1. Introducción

La transición hacia una energía más sostenible requiere sistemas de almacenamiento eficientes. Entre todas las opciones, las baterías de ion-litio son las más usadas por su alta capacidad, larga duración y rapidez para cargar y descargar. Con el crecimiento de energías renovables como la eólica y solar, que pronto llegarán a 510 GW instalados [1], la demanda de sistemas de almacenamiento fiables aumenta. Estas baterías no solo almacenan energía para la red, sino que también alimentan vehículos eléctricos, híbridos, autobuses y scooters. Por eso, optimizar su rendimiento y seguridad es un desafío clave para la ingeniería actual.

El funcionamiento y la seguridad de las baterías de ion-litio dependen en gran medida de parámetros como la tensión de circuito abierto (OCV), la resistencia interna (R1, R2) y la capacitancia (C). Estos parámetros varían de forma no lineal según el estado de carga (SOC), la temperatura y el estado de salud (SOH) de la batería. Por ello, estimarlos con precisión en condiciones reales es clave para diseñar sistemas de gestión eficientes (BMS), prolongar la vida útil y prevenir fallos. Normalmente, los fabricantes emplean cicladores comerciales para obtener estos datos, pero su coste a veces puede superar los 25.000 dólares [2], lo que dificulta su acceso en laboratorios pequeños y académicos.

Este estudio presenta una metodología práctica y económica para probar tanto una sola celda como grupos de celdas en paralelo, usando bancadas compuestas con components accesibles (fáciles de replicar). hacer más accesible la investigación, esta tesis aborda otra limitación: la falta de pruebas y modelos para configuraciones a nivel de paralelo, módulo y pack. La mayoría de los datos disponibles solo cubren celdas individuales, generalmente de los fabricantes. Por eso, este trabajo desarrolla y valida un modelo escalable que usa circuitos equivalentes (ECM) y estimaciones de SOC para ampliar los parámetros de una celda a conjuntos mayores.

2. Estado del arte

Para simular el comportamiento eléctrico de las baterías de ion-litio, se usan modelos de circuito equivalente (ECM). Estos modelos representan la batería con resistencias y condensadores, simulando su respuesta al conectarla a una carga. Entre los modelos más comunes, el circuito equivalente de Thevenin de primer orden (ver Figura 1) ofrece un buen equilibrio entre simplicidad y precisión [3]. La resistencia R1 refleja la caída de tensión instantánea al aplicar una carga, mientras que R2 y C representan los efectos de polarización y la respuesta dinámica de la celda. Para obtener estos parámetros como función del estado de carga (SOC), se utiliza la Técnica de Valoración Galvanostática Intermitente (GITT), propuesta por Liu et al. [3].

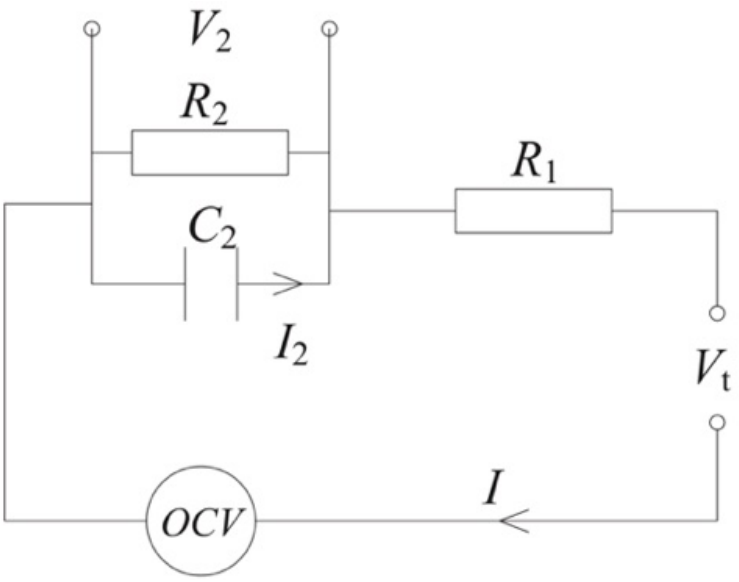


Figura 1: Modelo de circuito equivalente de Thevenin de primer orden [3]

Como se muestra en la Figura 2, la GITT consiste en descargar la celda con pulsos de corriente constante (en este caso, 18 A), seguidos de periodos de reposo. Durante estos descansos, la tensión en bornes asciende de forma exponencial hasta acercarse a la tensión en circuito abierto (OCV), lo que permite ajustar los componentes del modelo ECM a partir de la respuesta observada siguiendo las siguientes ecuaciones:

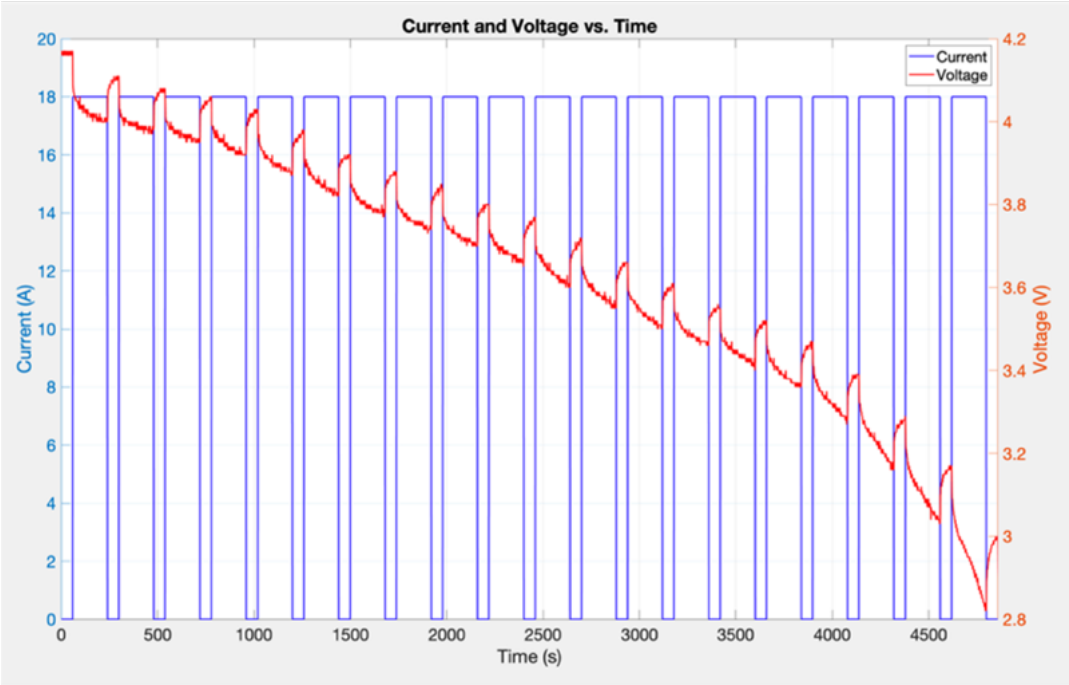


Figura 2: Corriente, Tensión vs Tiempo para un ciclo GITT a 1C [3]

$$R1\ (SOC) = \frac{V_0(0+) - V_0(0-)}{I}$$

OCV, R2 y C2 se calculan ajustando exponencialmente la caída de tensión desde V0, (instante justo después del corte de corriente) hasta V1, que corresponde a la tensión 60 segundos después de la desconexión:

$$v(t) = a * e^{-bt} + c$$

$$OCV\ (SOC) = c$$

$$R2(SOC) = a/I$$

$$C2(SOC) = 1/(R2 * b)$$

La Figura 3 muestra un detalle de dos periodos de desconexión, donde se observa el salto instantáneo ($I \cdot R_1$) y el comportamiento transitorio de modelado por R_2 y C).

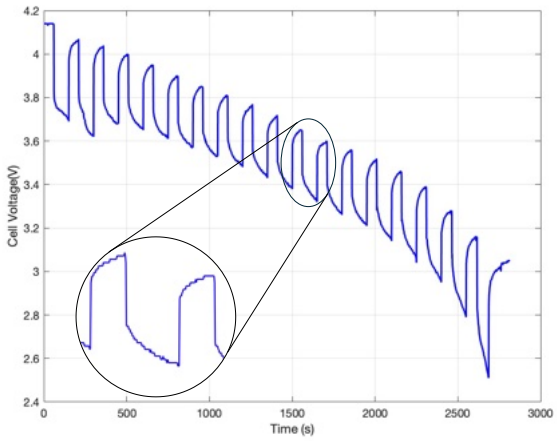


Figura 3: Detalle de la tensión en los bornes de la celda durante un ensayo GITT a 1C.

La celda se desconecta de la carga cada 5 % del estado de carga (SOC), lo que da lugar a 20 periodos de relajación a lo largo de una descarga completa [4]. Antes de pasar a la descripción experimental, conviene aclarar el concepto de SOC. El estado de carga representa la relación entre la capacidad restante y la capacidad nominal de la celda. Como no se puede medir directamente, debe estimarse. Una forma habitual de hacerlo es mediante el contador de Coulomb, que consiste en integrar la corriente a lo largo del tiempo. Aunque es un método sencillo, puede acumular errores por la deriva de los sensores y por incertidumbres en el valor inicial del SOC [5]. Como alternativa, los métodos basados en modelos, como el filtro de Kalman, permiten estimaciones más precisas [6]. Este filtro combina en tiempo real las mediciones de tensión y corriente con un modelo de circuito equivalente (ECM), actualizando el SOC continuamente y reduciendo la deriva, lo que lo hace especialmente eficaz en condiciones de carga dinámica.

3. Descripción experimental

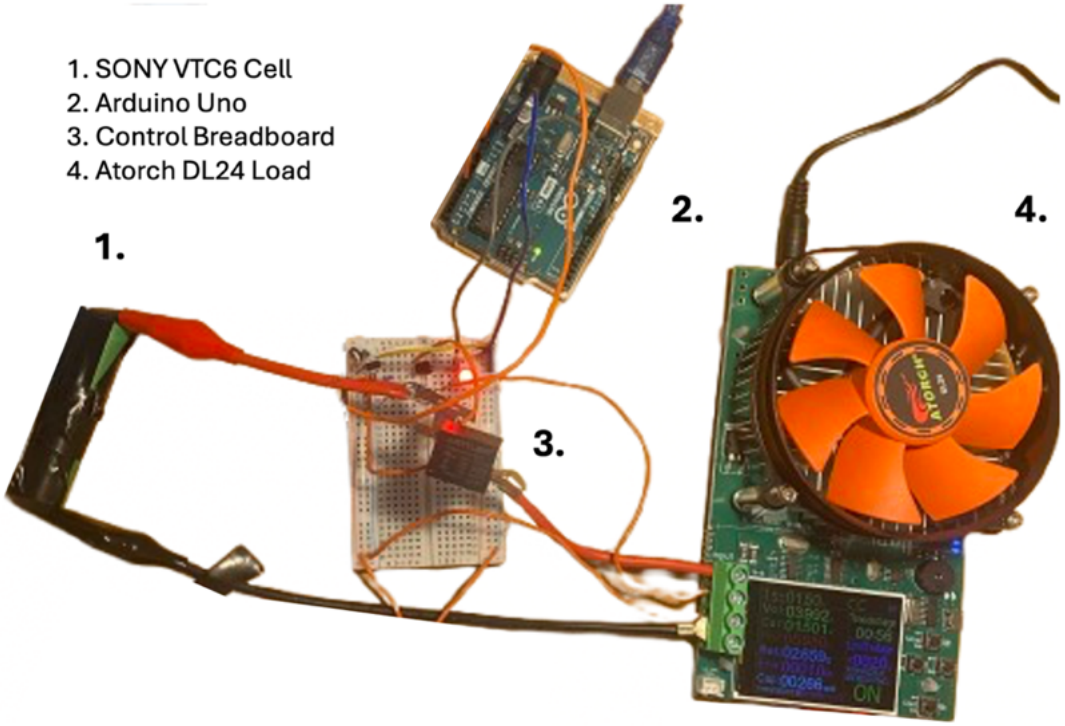


Figura 4: Bancada de baterías para celda VTC6 18650

La Figura 4 muestra el banco de pruebas para una sola celda, que utiliza un Arduino Uno como microcontrolador y un Atorch DL24 como carga programable. El Arduino controla los ciclos de descarga, mide la tensión y la corriente, y desconecta la batería en caso de emergencia. El perfil GITT se ejecuta con un relé de potencia. El sistema permite descargas de hasta 20 A, con un margen de error en la regulación del corriente de ±0,01 A, y entrega hasta 180 W, suficiente para probar una celda 18650 hasta 6C.

Además de la bancada para una sola celda, se desarrolló otra de mayor potencia para probar seis celdas en paralelo (Figura 5). Este sistema incluye tres elementos principales: una resistencia variable, un bus bar de cobre y un Arduino MEGA 2560, que actúa como controlador y datalogger. Todas las conexiones se diseñaron para soportar corrientes hasta 54 A, remplazando el relé por un contactor TE Kilovac. Además, se añadieron sensores térmicos en la parte superior, central e inferior de cada celda, además de la carga y el ambiente. En lugar de los MOSFET, este sistema utiliza una carga de impedancia variable formada por 17 resistencias y 11 relés. Seis resistencias cerámicas manejan la mayor parte de la corriente y permanecen activadas, mientras que las demás se encienden según sea necesario para ajustar la resistencia total y regular la corriente durante la descarga.

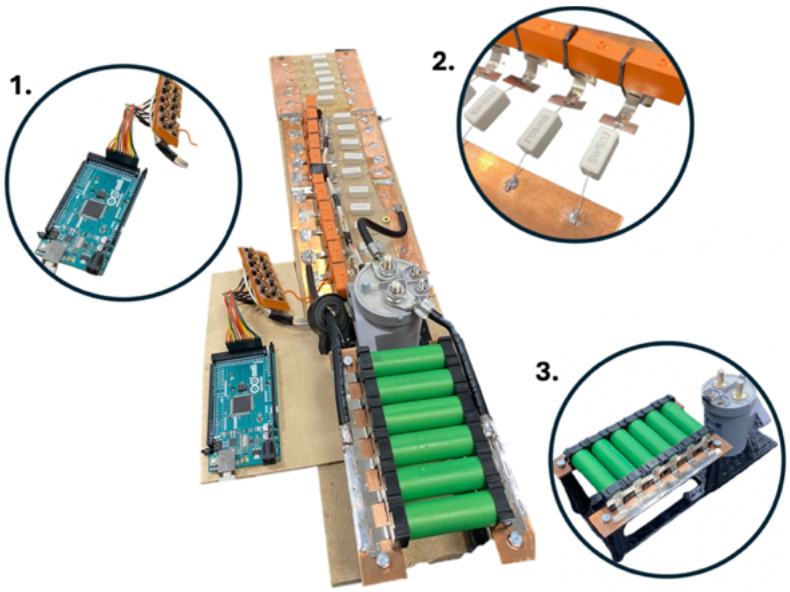


Figura 5: Bancada de baterías en paralelo

Este proyecto se centrará en un solo tipo de célula: la SONY-MURATA US18650VTC6 (3000 mAh). Se eligió por ser una de las celdas cilíndricas más comunes, contar con numerosos estudios similares de referencia y tener un bajo coste, adecuado al presupuesto del proyecto. Las células se descargaron a 0,5C, 1C, 2C y 3C, tanto a nivel de celda como en paralelo, realizando tres intentos por cada curva descarga.

4. Resultados

Después de completar todos los ciclos de descarga, se calcularon los valores de OCV, R1, R2 y C en cada desconexión. La Figura 6a muestra el perfil promedio de OCV frente a SOC para una celda única a distintos *C-rate*. Se observa que, para un mismo SOC, el OCV baja al aumentar la velocidad de descarga. Por ejemplo, a 3C el OCV es unos 0,15 V menor que a 0,5C en el rango medio de SOC, lo que reduce la energía disponible en celdas individuales. También, para todo *C-rate*, la caída de tensión es mayor por debajo del 40 % de SOC. Esta 'rodilla' sugiere que en el interior de la celda ocurre un cambio en las reacciones electroquímicas o posibles limitaciones en el transporte de iones cuando la celda se aproxima al final de su descarga. Las curvas de OCV se juntan a bajo SOC, lo que sugiere que el *C-rate* influye menos cuando el material de la celda está casi agotado. En el caso de la celda individual, la resistencia interna (R1) muestra una forma de U: es más alta al inicio (>95 % SOC) y al final (<20 % SOC) de la descarga, con un mínimo claro entre el 40 % y el 60 % de SOC (Figura 6b). Este comportamiento es el esperado. A SOC alto, los iones de litio están muy concentrados en el ánodo, lo que dificulta su movimiento.

a) b)

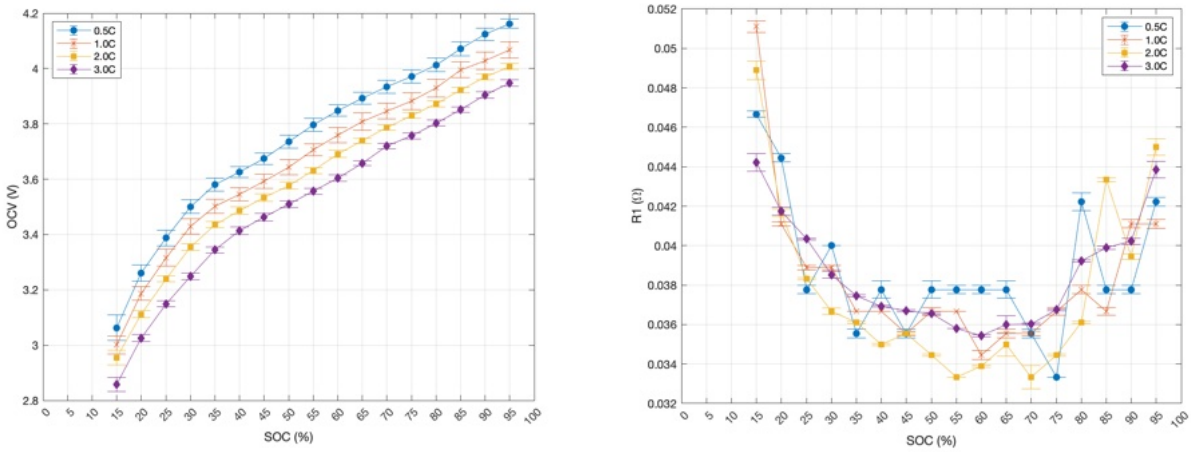


*Figura 6 a,b: D*ependencia de la tasa de descarga en el comportamiento dinámico de una celda individual bajo ciclos GITT: a) OCV (V) vs SOC (%), b) R1 (Ω) vs SOC (%).

A SOC bajo, ocurre un fenómeno parecido cátodo, al haber pocos espacios libres para los iones restantes, la resistencia incrementa también al final de la descarga. La Figura 7 muestra cómo varían los parámetros del modelo ECM al conectar las celdas en paralelo. En la Figura 7a, todas las curvas OCV-SOC tienen una pendiente similar (~0,01 V/% SOC) al inicio de la descarga, aunque las curvas de 2C y 3C están desplazadas hacia abajo unos 0,05 V y 0,1 V, respectivamente. Por debajo del 40 % de SOC, el voltaje cae con más rapidez, y todas las curvas se agrupan entre 2,85 V y 2,95 V cerca del 15 % de SOC. En cuanto a R1, la configuración en paralelo presenta valores medios mucho más bajos (entre 0,006 y 0,002 Ω), pero también más ruido y oscilaciones por encima del 30 % de SOC, probablemente debido a limitaciones en la resolución de las mediciones de tensión.

a) b)

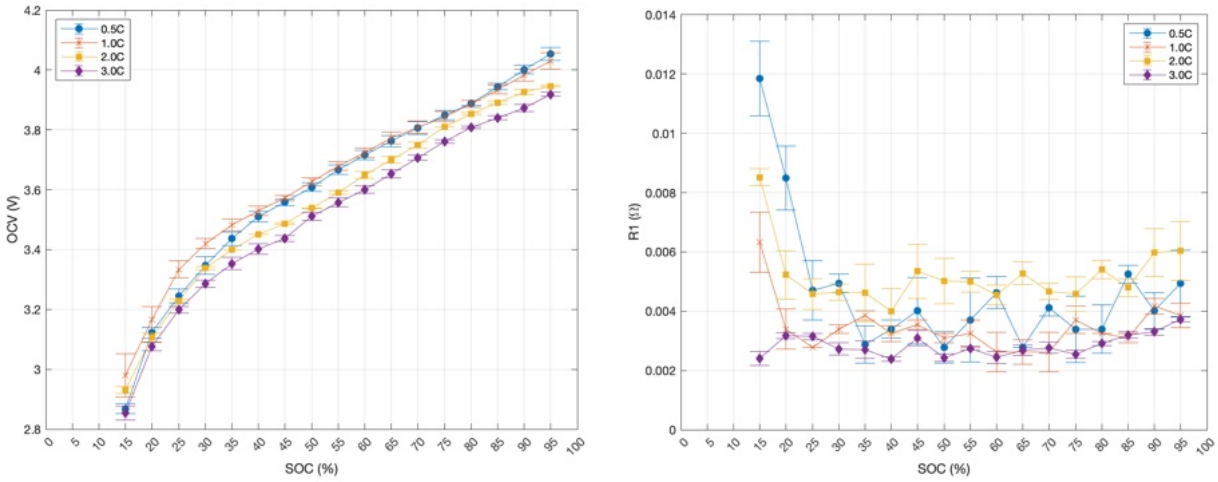


Figura 7 a,b: *Dependencia de la tasa de descarga en el comportamiento dinámico de un paralelo de 6 celdas bajo ciclos GITT: a) OCV (V) vs SOC (%), b) R1 (Ω) vs SOC (%).*

Tras procesar los resultados del ECM para la celda individual y el conjunto en paralelo, se realizó un análisis comparativo para evaluar cómo escalan los modelos. El perfil SOC-OCV mantuvo coherencia al escalar de una celda a 6 en paralelo. Sin embargo, la impedancia y la capacitancia internas mostraron mayor variabilidad. Por ejemplo, la impedancia en paralelo fue 17 veces menor (cuando según la literatura debería ser solo 6 veces menor). Por otro lado, la capacitancia fue entre 100 y 1.000 veces mayor de lo previsto. Estas diferencias reflejan la dificultad de escalar el comportamiento transitorio y las limitaciones del sistema de medición. El uso de un ADC de 10 bits en el Arduino, con un error de ±4,9 mV, dificultó captar con precisión la respuesta transitoria (~50 mV) necesaria para estimar parámetros como R2 y C. Además, separar R2 y C resultó complicado, ya que ambos son muy sensibles durante el ajuste exponencial. Analizar directamente la constante de tiempo habría sido un método más sencillo y fiable, al evitar la dependencia del peso relativo entre R2 y C en el ajuste.

5. Escalado de los modelos de batería

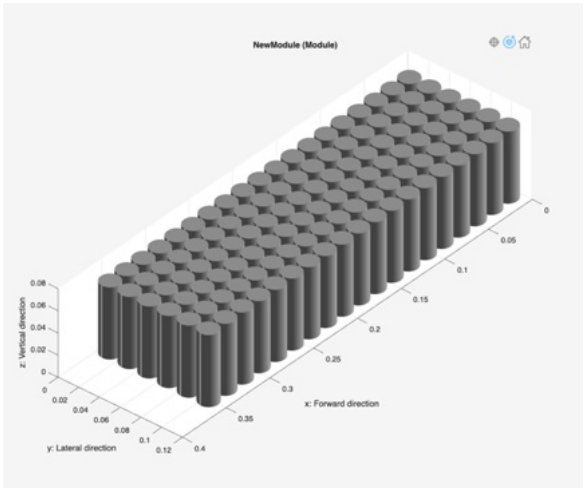


Figura 8: Modelo en Simscape de la batería del monoplaza Formula Student IFS-06

A partir de los parámetros del ECM para una sola celda, se construyó un modelo en Simscape (MATLAB), que posteriormente se escaló a nivel de paralelo, módulo (como se muestra en la Figura 8) y *pack* completo. Luego, el *pack* fue sometido a pruebas de esfuerzo con tasas de descarga de 0,5C, 1C, 2C y 3C, donde se comparó perfiles de tensión, OCV, temperatura y SOC. Para simular un uso real en un vehículo eléctrico, el modelo completo del pack se sometió al ciclo de conducción urbana FTP-75, disponible en la biblioteca de ciclos estandarizados de Simscape. Este ciclo incluye arranques y paradas frecuentes, y ofrece una visión más realista del comportamiento del pack en condiciones de conducción urbana. Para simplificar el análisis, se excluyó el frenado regenerativo. La Figura 9 muestra la corriente y la tensión del pack durante el ciclo de conducción urbana, FTP-75.

a) b)

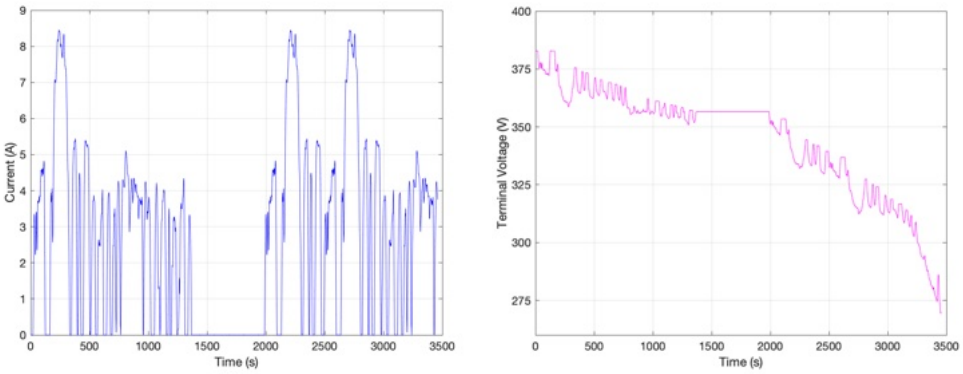


Figura 9): Simulación ciclo de conducción FTP-75 en el pack de baterías del Formula Student IFS-06: a) Corriente (A) vs Tiempo (s), b) Tensión (V) vs Tiempo (s)

6. Riesgo de fuego

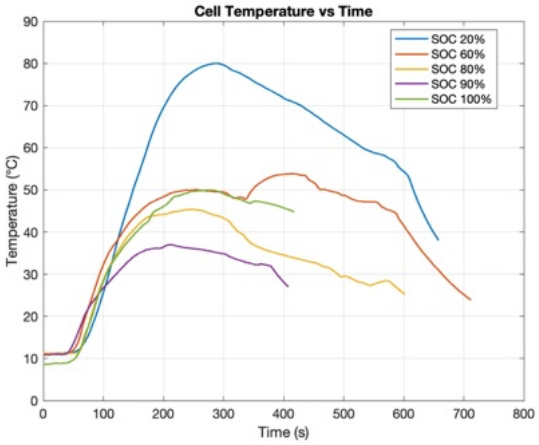


Figura 10: Temperatura Celda VTC6 (Celsius) vs Tiempo(s) tras cortocircuito

Después de completar todos los ciclos, las celdas Sony-Murata VTC6 18650 se sometieron a pruebas de cortocircuito para estudiar el embalamiento térmico. El objetivo fue analizar cómo el estado de carga (SOC) afecta la probabilidad y gravedad del embalamiento. Se probaron cinco celdas con SOC de 20%, 60%, 80%, 90% y 100% usando cortocircuito externo. Ninguna de las celdas mostró embalamiento térmico. La temperatura más alta registrada fue 80 °C en la celda con 20% SOC, que no ventiló, probablemente porque su pestaña de seguridad permaneció intacta, permitiendo que el calor y la presión interna aumentaran debido al gas generado en la reacción. En las demás celdas se observó ventilación de gas, lo que probablemente alivió la presión interna y evitó un aumento mayor de temperatura. Se puede concluir que la ventilación actuó como un mecanismo de seguridad que previno el embalamiento térmico. Es importante destacar que las pruebas se realizaron al aire libre a 10 °C, lo que posiblemente también contribuyó a que las celdas no entraran en embalamiento térmico.

7. Conclusión

Este estudio presenta un método práctico y económico para caracterizar baterías, con dos bancos de pruebas hechos a medida: uno para celdas individuales y otro para configuraciones en paralelo de seis celdas. Ambos pueden realizar descargas GITT hasta 3C (20 A y 54 A respectivamente), utilizando dos formas de controlar la corriente: una resistencia variable con MOSFET y un conjunto de 17 resistencias controladas por relés para corrientes más altas. Se obtuvieron parámetros electroquímicos clave (OCV, R1, R2, C) a diferentes tasas de descarga, y se crearon modelos de circuito equivalente para celdas simples y en paralelo. Los perfiles OCV-SOC escalaron bien de la celda individual al paralelo, pero la impedancia y la capacitancia interna presentaron tendencias no lineales en su escalado, requiriendo futuros trabajos para investigar en más profundidad su relación.

Con los datos de una sola celda, se creó una base ECM que se integró en MATLAB Simscape para simulaciones rápidas y escalables, validadas con el ciclo de conducción FTP-75 en un pack 95S6P de un coche de Fórmula Student. Las pruebas destructivas de cortocircuito no causaron embalamiento térmico. Las celdas que ventilaban limitaron la subida de temperatura, mientras que la celda con 20% SOC fue la que más se calentó por no ventilar. En resumen, este trabajo ofrece un método completo y accesible para caracterizar celdas 18650 de litio y escalar modelos ECM, dando herramientas útiles para investigadores académicos y pequeños proyectos industriales.

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1. Introduction

In a world increasingly powered by electricity, batteries are at the core of this transformation. With 510 GW of installed renewable capacity [1], renewables are quickly surpassing fossil fuel production. However, renewables face a significant challenge: energy is often not generated on demand, making energy storage systems crucial for storing excess power until the grid requires it. Among all battery types, lithium-ion batteries have become the most widely used due to their long-life cycle, compact size, light weight, fast charging, and low self-discharge rates [2]. Beyond grid solutions, lithium-ion batteries are found in electric vehicles (EVs), plug-in hybrids (PHEVs), and everything from buses to scooters. They play a critical role in our daily life, making it essential to optimize the battery performance through precise characterization of the electrical, thermal models and battery management systems (BMS). In this context, this paper will focus on developing and validating a practical approach to testing li-ion cells, developing an electrochemical cell model (ECM) and State of Charge (SOC) model to optimize battery performance and enhance battery longevity.

1.1 *A brief introduction to electrical vehicles*

Electric vehicles (EVs) are among the most prominent forms of transportation in today's society. Currently, over 40 million EVs are in operation globally [3], with 17 million projected to be sold in 2024. Their history surprisingly dates back to the 1830s, even before the invention of the internal combustion engine vehicles (ICE). Early EV prototypes faced substantial challenges: their batteries were non-rechargeable, some even used disposable crude oil batteries, and their powertrains were highly inefficient, making them no match for internal combustion engine vehicles (ICEV). However, advancements in battery and powertrain technology over time have made EVs increasingly viable. Additionally, as public awareness of global warming and climate change grows, electric cars are becoming more integrated into society, paving the way for sustainable transportation. EVs offer several advantages over ICEVs, including more efficient transmissions, higher energy density, and great charge and discharge power. Despite these benefits, the adoption of EVs on a mass scale is still limited by current battery technology and the scarcity of rare metals required to manufacture EVs. One of the biggest challenges is studying cell modelling and how its model changes with time and degradation. Estimating a cell's lifespan requires testing across hundreds, if not thousands, of charge and discharge cycles. While efforts have been made to make these tests more accessible, they remain costly and not readily available. Continued research in battery modelling is therefore essential to optimize battery life, peak performance, and range, all of which are critical factors for enabling EVs to fully replace ICEVs.

2. State of the art

2.1 *Battery components*

The battery is a fundamental component of the powertrain system in any electric vehicle (EV). It comprises a series of cells that can be connected in both series and parallel configurations to form a module *(Figure 1)*.

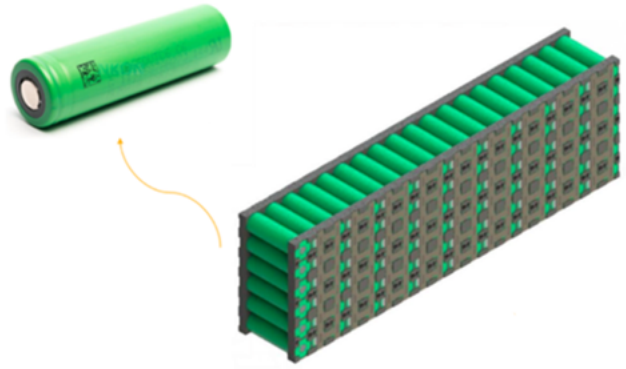


Figure 1: Battery module and cell from a Formula Student race car

These modules are then assembled in series to form a battery pack, and then packaged in a protective enclosure, commonly referred to as accumulator (*Figure 2 & Figure 3)*.

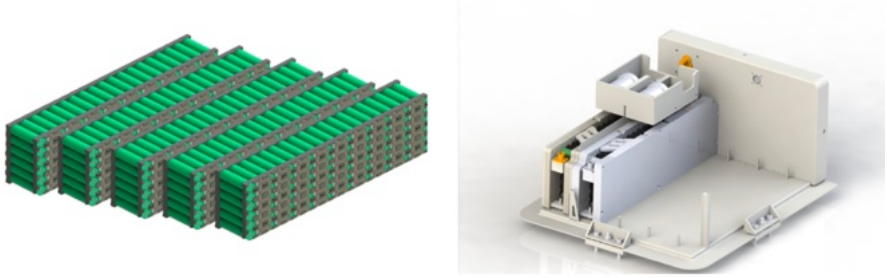


Figure 2: Battery pack configuration and accumulator from a Formula Student race car

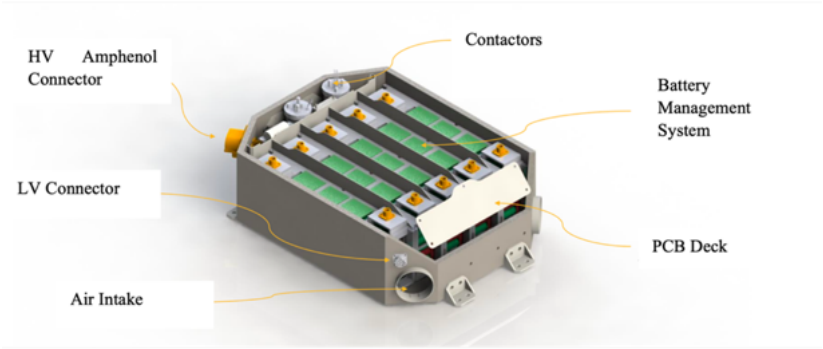


Figure 3: Battery pack from a Formula Student race car

The configuration of cells and modules can vary depending on the desired characteristics of the battery. There are also different types of cells: cylindrical, pouch, and prismatic (*Figure 4)*.



Figure 4: Cylindrical, pouch and prismatic cell

The chemical composition of cells can vary, but they typically consist of a graphite anode, a metal oxide cathode, and a lithium-ion electrolyte. Cells are usually characterized by the type of metal oxide cathode that they have, as this what is usually changed to produce different voltage potential and energy storage capacities. However, a detailed discussion of cell chemistry goes beyond the scope of this research. In addition to the cells and modules, batteries include other electronic components that monitor critical parameters like temperature, cell voltage, current, and insulation. These components form the Battery Management System (BMS) (see Figure 4*)*. The BMS ensures the cells operate within their nominal range, and in the event of a failure, it disconnects the battery and informs the operator.

2.2 *Battery modelling and testing*

Understanding the electrochemical behavior of a battery cell is crucial for designing battery packs, modeling their lifespan, and identifying failure mechanisms to develop effective battery management systems (BMS). BMS software typically uses an equivalent circuit model (ECM) to represent the cell, which relies on parameters such as State of Charge (SOC), Open Circuit Voltage (OCV), and internal cell impedance. A key challenge in building the ECM is that SOC, OCV, and internal impedance cannot be directly measured under load; instead, they must be computed using current and terminal voltage as inputs. Before exploring how these models are calculated, it is important to first define SOC and OCV. The State of Charge (SOC) of a battery is the amount of charge available at a particular time relative to its total capacity when fully charged [4]. As current is drawn from the battery, the cells discharge, causing the SOC to decrease until no charge remains. SOC is influenced not only by current draw but also by factors such as temperature and the overall health of the battery, which will be explored further in later

sections. Open Circuit Voltage (OCV) is the voltage measured at a cell's terminals when it is not under load. As the cell discharges, the OCV decreases due to the narrowing potential difference between the anode and cathode. Additionally, OCV can be modeled as a function of SOC. While various models exist, detailed OCV vs. SOC modeling falls outside the scope of this work.

2.2.1 Equivalent circuit model

To develop an equivalent circuit model that predicts both the dynamic and static electrochemical behavior of cells, it is essential to characterize Open Circuit Voltage (OCV) and internal impedance as functions of State of Charge (SOC). Open Circuit Voltage and internal impedance as function of State of Charge. Hu et al. [5] compared 12 equivalent circuit models, evaluating both complexity and accuracy. They concluded that the most effective method involved using a first order Thevenin model (see Fig. 1), which uses a combination of resistances and RC time constants series to capture the instantaneous and dynamic behavior of the cells, where R1 represent the ohmic resistance and R2 and C2 represent the electrochemical reaction [6].

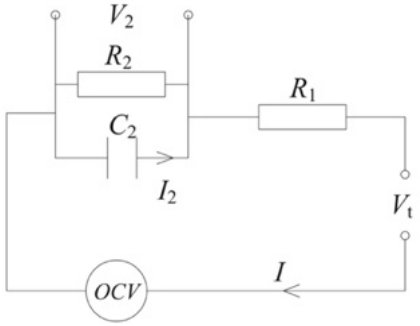


Figure 5: First order Thevenin Equivalent Circuit Model [6]

To determine the parameters R1, R2, C, and OCV as functions of SOC, various tests involve cycling the batteries (discharging/charging at specific rates) over different intervals and C-rates.

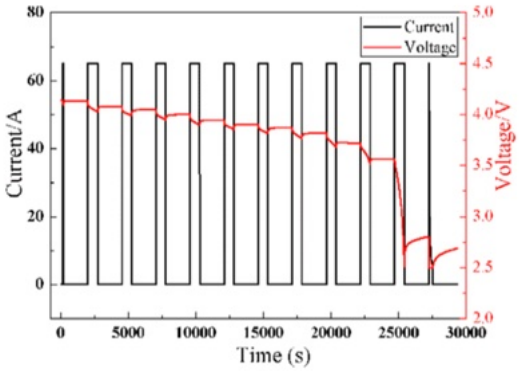


Figure 6: Current (A) vs Time (s) profile of a GITT discharge cycle [6]

This paper will focus on using the Galvanostatic Intermittent Titration Technique (GITT), as proposed by Liu et al. [6], which offers a good balance between curve complexity and accuracy. The GITT consist of discharging the battery a pulse at a constant current C-rate followed by a relaxation period, where no current passes through the battery, the voltage levels out and reaches the steady state. Figure 6 illustrates a typical GITT discharge curve. The current remains at a constant C-rate for a predetermined duration, often corresponding to a specific SOC jump (for example, the time it takes to discharge 5% SOC). After this period, the load is disconnected, allowing the voltage to evolve to its steady state. The load is then reconnected for the same duration, and this process is repeated until the battery is completely discharged.

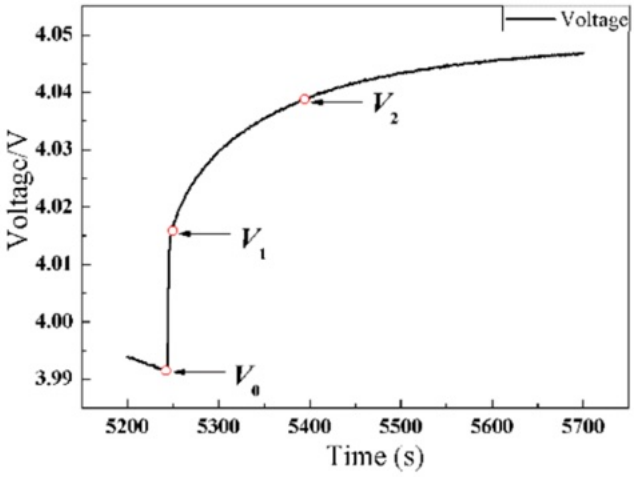


Figure 7: Close-up relaxation period after a disconnection at 80% SOC [6]

Figure 7 shows close-up view of one the relaxation periods shown in Figure 6. Immediately after the load is disconnected, there is an instantaneous voltage jump. This jump is modeled by R1, the ohmic resistance of the cell. To calculate R1 for a specific SOC%, $V_0(0-)$, is used which represents the voltage just before disconnection, and $V_0(0+)$, the voltage immediately after disconnection, divided by the current I:

$$R1\ (SOC) = \frac{V_0(0+) - V_0(0-)}{I}$$

OCV, R2, C2 are calculated using an exponential fit of the voltage from $V_0(0+)$ to V_1, which is the voltage 60s after the disconnect:

$$v(t) = a * e^{-bt} + c$$

$$OCV\ (SOC) = c$$

$$R2(SOC) = a/I$$

$$C2(SOC) = 1/(R2 * b)$$

For each disconnection, R1, R2, C2, and OCV are obtained as functions of SOC. To characterize these parameters at every 5% SOC interval, a constant current pulse is applied for the duration of each 5% SOC drop. Note that this duration will change depending on C rate. For example, for C=1C, a 5% will last around 3 minutes. This process results in a total of 20 disconnections when discharging the battery from 100% to 0% SOC.

2.2.2 State of Charge

Once R1, R2, C, and OCV have been determined for different SOC values, the next step is to estimate SOC. Several methods exist for determining the relative amount of charge remaining in a cell. This paper will discuss the most relevant approaches, including Coulomb counting and various iterations of the Kalman filter.

The first method: Coulomb counting, counts the charge change as e^- move from the anode to cathode an vice versa. The SOC using Coulomb counting is given by:

$$SOC(t) = SOC(t-1) + \frac{\int_{t-1}^{t} -I(t)dt}{3600 * Q_{nom}}$$

In this equation, $SOC(t-1)$ represents the previously recorded State of Charge, I(t) is the current during the specified time period, and Q is the nominal cell capacity. Note that the sign convention used defines positive current during cell discharge and negative current during charging. As a result, the current in the integrator is assigned a negative sign. Using Laplace block notation to represent this equation:

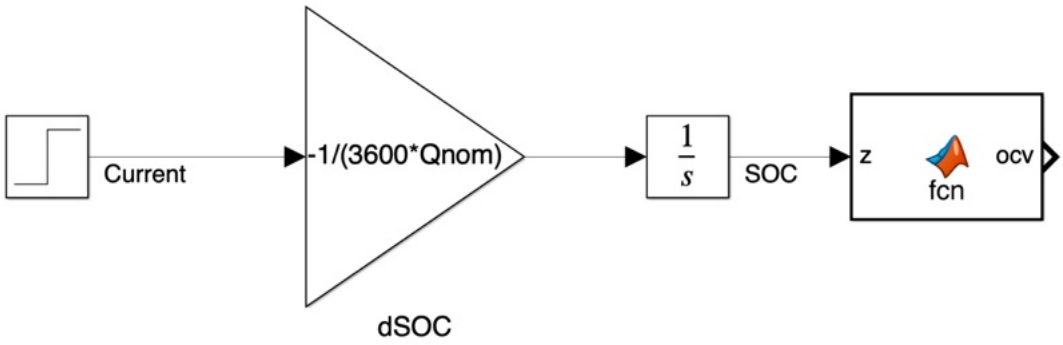


Figure 8: Simulink Laplace block diagram SOC coupled with OCV=f(SOC)

Combining the SOC calculation with the equivalent circuit model, the SOC value can be used to determine the OCV and calculate terminal voltage (Vt) using the internal impedance (R) and current (I). Figure 9 shows the Laplace block notation implemented Simulink to calculate terminal cell voltage.

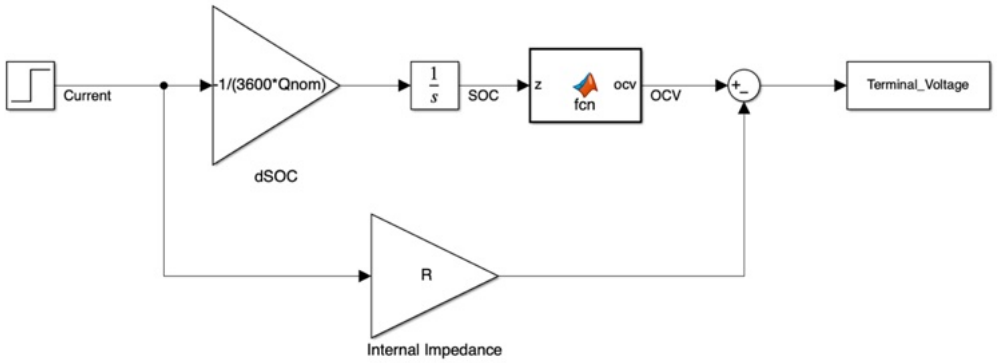


Figure 9: Equivalent circuit model coupled with OCV=f(SOC)

One of the main limitations of Coulomb counting is its strong dependence on the accuracy of the initial SOC estimate and the measurement noise of the current sensor. Essentially, the Coulomb counter integrates the current to determine changes in the battery's charge [7]. However, any measurement errors accumulate over time, causing the estimation to drift further from the true value with each cycle. If the initial estimate is incorrect, the Coulomb counter will maintain an offset throughout the entire discharge process. This issue can be solved using other model-based techniques like Kalman filters, which combines mathematical models with real-time data to minimize SOC estimation error.

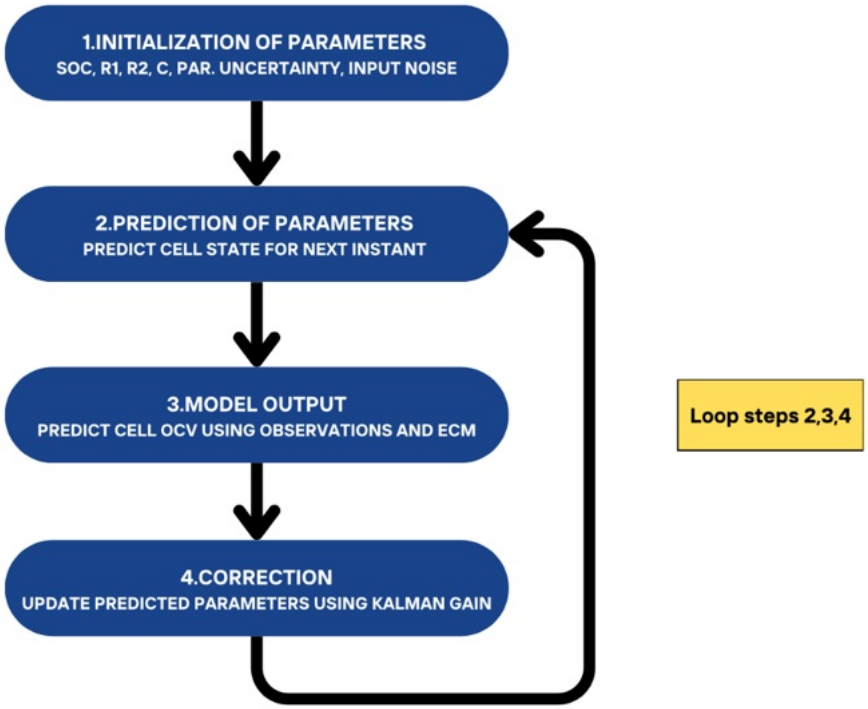


Figure 10: Simplified Kalman Filter Flowchart

As presented in Figure 10, the Kalman Filter is initialized with estimated initial values for SOC, R1, R2, and C, along with the uncertainty for each condition and the input noise. After initialization, the cell parameters for the next instant t_{k+1} are predicted. Using multiple current, voltage, and temperature measurements, the parameters are then calculated based using the ECM model. Finally, the parameters derived from the observations are compared to the predictions, and the error is calculated. The error between the observed and predicted parameters is then corrected using the Kalman gain, repeating cycle time after time for every instant as shown in Figure 10.

Various types of Kalman filters can be used to estimate State of Charge (SOC) or State of Health (SOH) by combining predictions with observations. This paper will start with an SOC estimator using a basic Kalman filter, followed by a detailed examination of its variations, including the Extended Kalman Filter (EKF), Adaptive Extended Kalman Filter (AEKF), and Unscented Kalman Filter (UKF) [8].

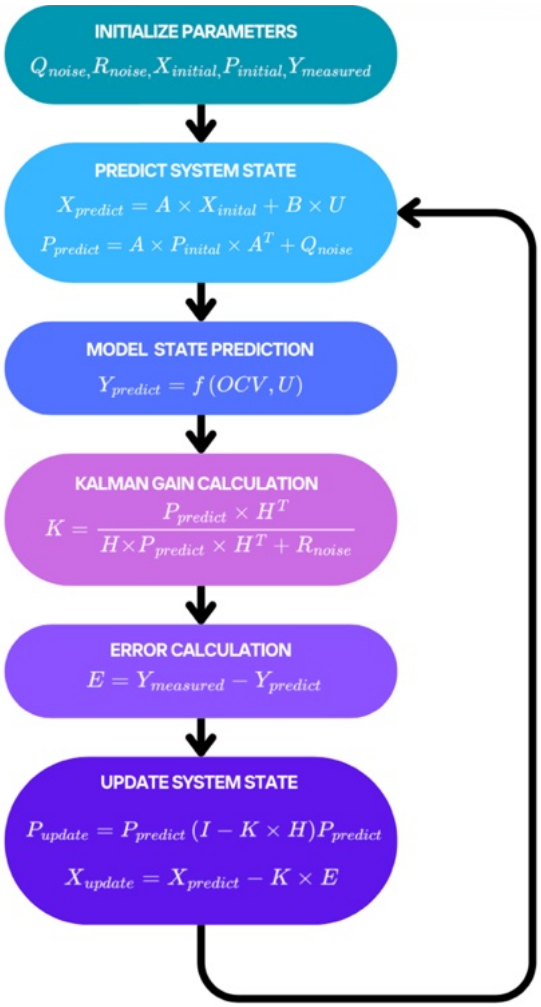


Figure 11: Standard Kalman Filter Flowchart

As shown in Figure 11, an initial value is assigned to all the parameters of the Kalman filter. The process noise covariance, Q_{noise}, represents the uncertainty originating from the process noise. Similarly, the measurement noise covariance, R_{noise}, represents the uncertainty associated with the observations. Moreover, initial state estimate is also assigned for SOC, $X_{initial}$, and set $P_{initial}$, the covariance, which represents the uncertainty of this initial estimate. $Y_{measured}$, is the initial open cell voltage observed.

Once the Kalman filter is initialized, the system state, $X_{initial}$, is predicted using state-space equations. In this step, the current state X_n (which is $X_{initial}$ in the first iteration), is known, and the state transition matrix A, is applied to model how the state evolves in the next iteration based on the previous state. The control matrix B accounts for changes in the state due to external variables. With these, the system state, $X_{predict}$ is calculated, and $P_{predict}$ is updated. Note that $P_{predict}$ is the state covariance, which represents the predicted uncertainty after propagation.

Next, in step 3, the model state prediction is performed. Here, using the equivalent circuit model (ECM) introduced in section 2.2.1, a prediction for OCV is calculated based on the predicted SOC value. In step 4, the value of the Kalman gain is calculated using $P_{predict}$, R_{noise} and H, where H is the Jacobian of the function OCV=f(SOC). The error is then calculated as the difference between the predicted and measured OCV. Finally, in step 6, the system state is updated. Using the Kalman gain, prediction is adjusted based on how much certainty there is in the observation versus the prediction. This correction reduces uncertainty, updating both P_{update} and X_{update}, which then become $P_{initial}$ and $X_{initial}$ for the next iteration.

2.2.3 Thermal behaviour and modelling

Thermal behavior is a key aspect of any cell model. Due to internal impedance and exothermic processes, heat is generated during battery operation. The temperature at the cell's core can be several degrees higher than at its surface. Additionally, temperature gradients can also occur across the cell surface, though they are typically much smaller compared to those in the core. Typically, the core temperature is not monitored because embedding sensors inside cells is a difficult challenging, although this has been done experimentally in the past by Forgez et al. [9]. Therefore, developing thermal models is crucial to monitor critical temperatures and ensure the cell operates within its safe range.Forgez et al [9], tested different equivalent circuit models of varying complexity to model the cell thermal behavior, comparing both complexity and accuracy. Figure 12a presents a more complex model designed for scenarios where both internal and external heat fluxes are explicitly considered in axial and radial directions. This model incorporates multiple heat transfer mechanisms, including convective and radiative

effects. However, a key limitation they encountered was the need for numerous additional measurements to determine all the necessary parameters, making it impractical for real-world applications. Forgez et al. [9] proposed a simplified equivalent circuit model, Figure 12b that estimates internal temperature using only a simple lateral surface measurement. One assumption made in this model is that the cell's surface temperature is uniform, which is not far from reality.

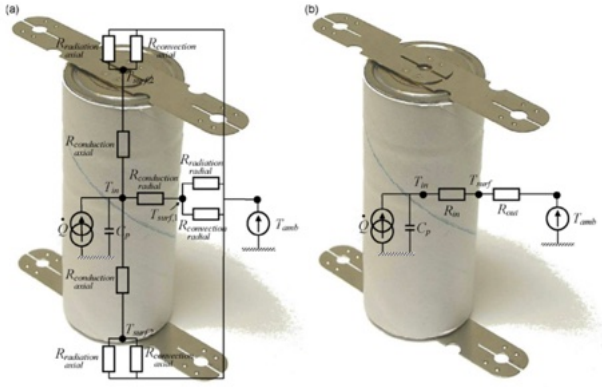


Figure 12 a,b: Equivalent circuit thermal model [9]

Using the simplified model, R_{out} parameter can be determined using a simple constant current pulse and measuring ambient temperature T_∞, surface temperature T_s, cell heat flux $\dot{Q}$ using the following expression:

$$R_{out} = \frac{T_s - T_\infty}{\dot{Q}}$$

To find the R_{in}/R_{out}, Forgez et al. [9] used an embedded thermocouple to find T_{in}, and determined the ratio using the following expression:

$$\frac{R_{in}}{R_{out}} = \frac{T_{in} - T_s}{T_s - T_\infty}$$

This approach is simple yet requires the previous characterization of the internal temperature using an embedded thermocouple which may not always be available. Interestingly Prabhakar et al. [10] proposed another equivalent circuit model that utilized the internal impedances characterized for electric model Prabhakar et al. [10] divided the heat generation into two phenomena: Ohmic heat for the internal impedance and polarization heat from the electrochemical reaction.

$$Q = Q_{ohm} + Q_p$$

Where Q_{ohm} was given by the internal impedance and Q_p was given by the first polarization resistance:

$$Q_{ohm} = I^2 \cdot R_1$$

$$Q_p = I^2 \cdot R_p$$

If all the heat leaves the core strictly in the axial or radial direction:

$$\dot{Q} = \frac{Q_{ohm} + Q_p}{A} \approx \frac{Q_{ohm} + Q_p}{2\pi r^2 + 2\pi r l}$$

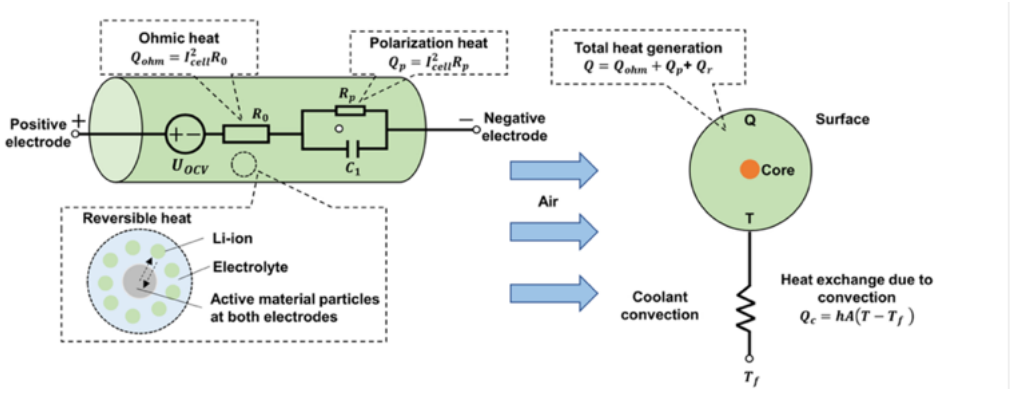


Figure 13: R-RC equivalent circuit thermal model [10]

2.3 *Fire safety*

During the normal operation of a battery, exothermic chemical reactions occur, generating heat that must be dissipated to prevent the battery's temperature from rising. The reaction rate of the battery follows Arrhenius's law, which depends exponentially on temperature, while the battery's cooling capacity follows Newton's law of cooling, which is linearly dependent on temperature. When the battery reaches a temperature known as the Thermal No-Return Temperature (TNR) [11], where the cooling system's dissipation capacity is exceeded, a chain of self-reinforcing reactions begins, potentially resulting in the ignition of the cell. This phenomenon is known as thermal runaway. This process, which occurs inside the cells, leads to the breakdown of various battery components and can result in a vehicle fire.

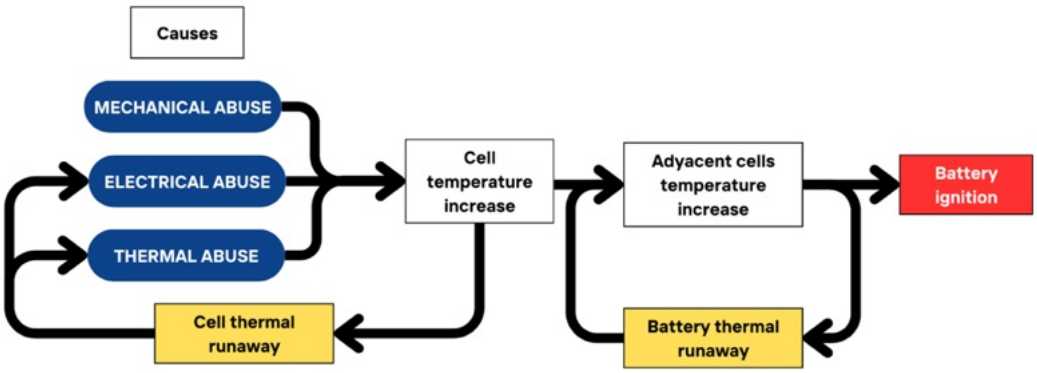


Figure 14: Thermal runaway causes simplified diagram

During thermal runaway, the cell's temperature increases exponentially, with no possibility of control. In addition to excessive temperature, thermal runaway can also occur due to mechanical or electrical abuse, for example, during an accident or because of overvoltage or a short circuit. Figure 14 shows a simplified diagram summarizing the causes and process of thermal runaway. The causes of fire will be examined in more detail in Section 2.3.4 and 2.3.5. As the temperature rises, the cell components begin to break down. This decomposition can lead to an internal short circuit between the cell's electrodes. A short circuit may cause sparks and the mixing of chemical components, whose decomposition triggers an exothermic reaction. This exothermic reaction, in turn, accelerates the cell's thermal runaway. Once the temperature reaches the point of no return, thermal runaway cannot be stopped. The rapid temperature increase in one cell can cause adjacent cells to enter thermal runaway, potentially igniting the battery.

2.3.1 Types of battery fires

Unlike fires in internal combustion engine vehicles (ICEVs), fires in electric vehicles (EVs) do not need an external oxygen source. The reaction within the cell itself supplies the fuel, oxygen, and heat required. Once the temperature reaches a sufficiently high level or a nearby ignition source is present, such as a spark from a shorted cell, gases released by the reaction initiate combustion, completing the fire triangle (Figure 15)



Figure 15: Fire triangle diagram

Case 1: Ignition of gases released by an external source. The cell's decomposition reaction produces oxygen and flammable, toxic gases [12] that inflate the cell (see **Error! Reference source not found.**). To prevent cell explosion, most manufacturers include a release valve that, upon reaching a certain pressure, allows the gases to vent outside. In the presence of any external spark, these gases ignite and begin combustion.

Case 2: Deflagration (Flash Fires) and unconfined vapor cloud explosions (UVCE). The accumulation of released gases in a poorly ventilated area can create explosive atmospheres. In this situation, a sudden ignition of the gas cloud or even an explosive deflagration (UVCE) may occur [13].

Case 3: Jet fires. If the cell's release valve malfunctions (or is absent), gases accumulate inside, causing the cell to swell. If a rupture occurs [14], a fire may start due to the release of a jet of flammable gas at high pressure [15]. This paper will not go into detail about explosive atmospheres; however, when dealing with battery fires it is crucial to always follow technical guide recommendations [16]. The IINST [17] provides additional information on the topic.

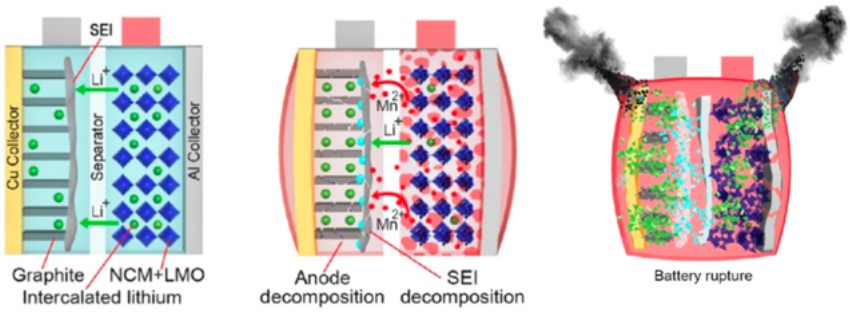


Figure 16: Cell decomposition process [16]

2.3.2 EV fire smoke and fumes composition

In addition to being flammable, the gases released from a battery fire are toxic. A study by the Royal Society of Chemistry [11] found that a large amount of H2, CO, CO2, CH4, C2H4, and C4H6 is released during an electric vehicle battery fire. These gases are highly toxic and explosive, which can complicate fire extinguishing efforts in poorly ventilated environments.

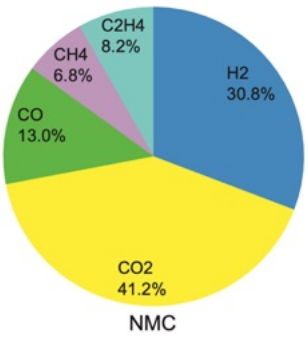


Figure 17: Toxic gases released during thermal runaway [11, 18]

2.3.3 EV fire re-ignition risk

Re-ignition occurs when a fire in an EV that was previously extinguished reignites. Since the decomposition reaction is exothermic, any remaining active chemical material can continue its exothermic process, raising the battery's temperature again and sparking a

new fire. A study by RISE (Research Institutes of Sweden) found that 5 out of 6 EV fires reignite after being extinguished [19]. In many cases, re-ignition occurs simply due to high temperatures; for instance, lithium batteries can reignite upon reaching 200°C again [14]. This phenomenon can occur hours, weeks, or even months after the fire is extinguished, so it is crucial to allow all active material to fully consume before putting out the fire and to monitor the battery in a secure environment.

2.3.4 Factors and causes of fires in EVs

Electrical abuse

Electrical abuses can be characterized into three types: short circuit, overcharge, and over-discharge. Under nominal conditions, a battery generates heat from two phenomena: the Joule effect due to current flow and the entropy change effect due to the exothermic chemical reaction. When a short circuit occurs between a cell's electrodes, a very high current flows, generating significant heat and burning the cell. Consequently, the temperature rises rapidly, often exceeding the critical temperature and triggering thermal runaway. Similarly, overcharge and over-discharge can lead to dendrite formation (solid electrolyte branches) in the battery, reducing battery capacity and potentially causing short circuits if they pierce the separator between the electrodes.

Thermal abuse

Thermal abuse can trigger thermal runaway if the cell surpasses the temperature of no return. As the temperature rises, at approximately 130°C, the separator decomposes, causing a short circuit between the electrodes. This short circuit further increases the temperature, leading to thermal runaway. Therefore, to prevent thermal runaway, it is essential to control and regulate the temperature to avoid the decomposition of any component, particularly the separator located between the electrodes. The following figure by Wang et al [20] summarizes how thermal abuse may cause thermal runaway.

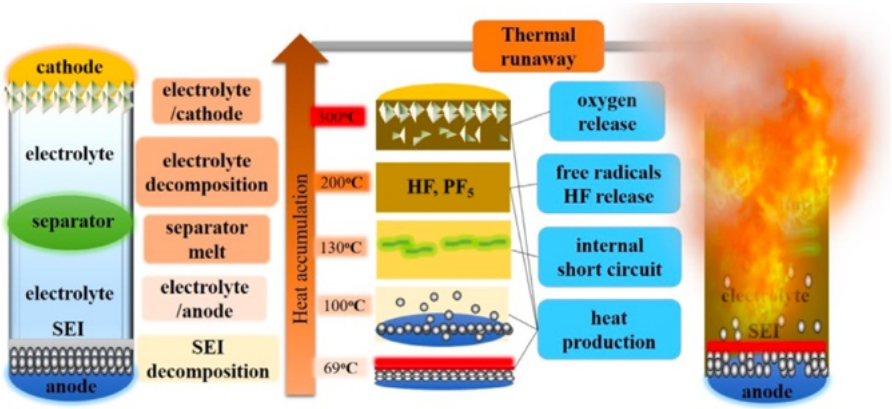


Figure 18: Thermal runaway caused by thermal abuse [20]

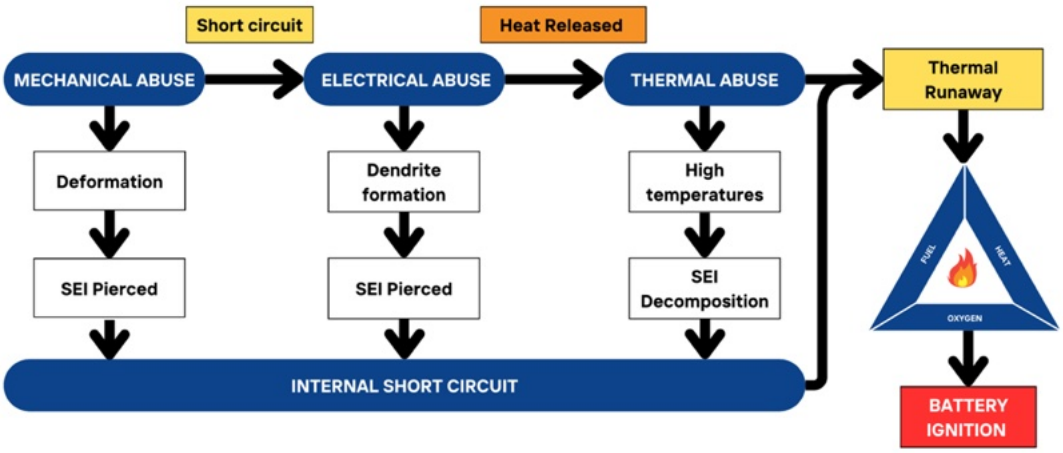


Figure 19: Battery fire mechanisms diagram

Mechanical abuse

Mechanical abuses occur when the battery experiences an impact, such as in a collision. Although batteries are generally well-protected within a safety casing, a high-speed impact or a manufacturing defect can cause cell deformation. This deformation can tear the separator, leading to a short circuit, generating heat, and potentially triggering thermal runaway. Figure 19 summarizes the three mechanisms that can cause a battery fire. As shown, internal short circuits are the common cause of thermal runaway.

2.3.5 Comparison between fires in EVs and ICEVs

Fire power and heat release rate

Current fire tests indicate that the heat release rate (HRR) is similar in both EVs and ICEVs. The peak heat release rate (PHRR) is around 9 MW and 5 MW for ICEVs and between 8 MW and 4 MW for EVs [21]. Figure 20a shows fire tests conducted by INERIS in France [22], with results similar to those obtained by the FPRF [21] (Figure 20b). However, fire power is more closely correlated with vehicle size and age than with whether the vehicle is an EV or ICEV.

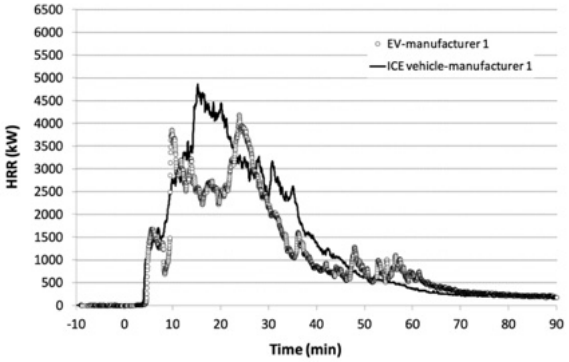


Figure 20a. EV vs ICEV HRR

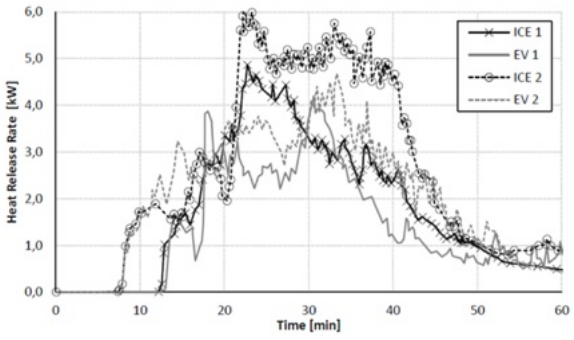


Figure 20b. EV vs ICEV HRR

The data in Figure 21a) was collected in a study by the FRPF [21], which conducted fire tests on ICEVs and EVs of varying sizes and weights. Additionally, both internal combustion vehicles (ICEVs) and electric vehicles (EVs) increasingly contain more plastics and other flammable materials. New-generation vehicles contain 91% more plastic than vehicles produced in 1970 [23]. This translates to a substantial increase in chemical potential energy, approximately 2300 MJ [24]. As seen in Figure 21b), this results in fires that spread more rapidly and have a higher peak power.

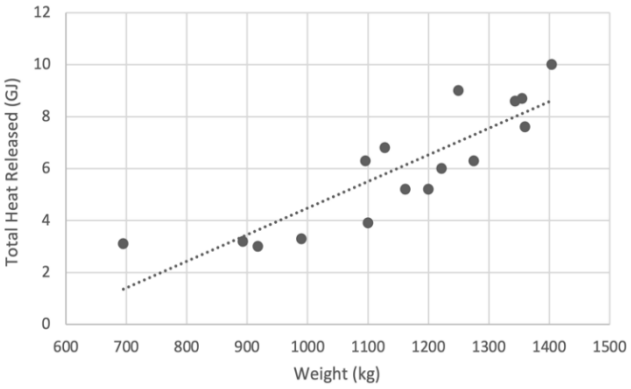


Figure 21a: Weight (kg) vs THR (GJ)

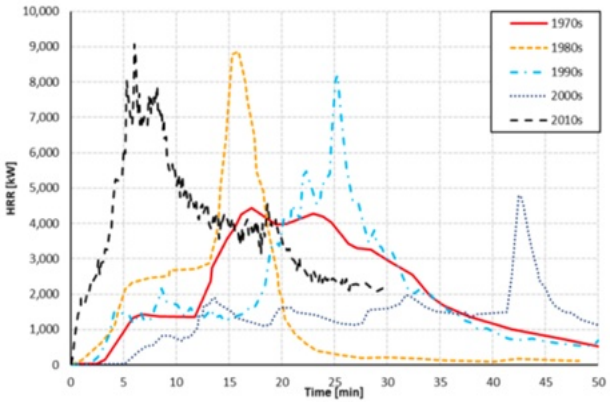


Figure 21b: HRR of cars different ages

Fire extinguishing time

A key factor to consider from a fire risk perspective is the effective fire extinguishing time. According to the NFPA (National Fire Protection Association), electric vehicles (EVs) have an extinguishing time ranging from 15 to 56 minutes for hybrids and 36 to 60 minutes for fully electric vehicles, compared to internal combustion engine vehicles (ICEVs), which take approximately five minutes to extinguish [25]. This is one of the main differences between fires in ICEVs and EVs. Although the heat release rate (HRR) may be similar, electric vehicle fires are not usually fully extinguished within 5 minutes. This is often because the extinguishing water does not reach the inner part of the battery, preventing the reversal of thermal runaway even if the fire in the vehicle body is extinguished. Consequently, EV fires require a larger amount of water compared to ICEVs. Other NFPA studies have found that more than 10,000 liters [26] and a flow rate of approximately 200 liters per minute are needed to extinguish an EV, compared to the 4,000 liters [27] required for an ICEV. However, this amount can vary significantly depending on the size of the electric vehicle, battery location, and extinguishing time. Additionally, the longer extinguishing time increases the risk of damage to building structures.

3. Description

3.1 *Experimental Description*

In industry, most Li-Ion cells are tested individually, with limited data available on their performance when connected in series or parallel within a pack. To address this gap, the following experimental procedure and test banks were developed to cycle cells both individually and in parallel. The aim is to investigate potential variations in internal impedance and capacity that may arise when cells are connected in parallel. The selected cell for testing is the SONY-MURATA INR US18650 VTC6 (3000 mAh), which uses INR ($LiNiMnCoO_2$) chemistry. This cell was chosen due to its widespread availability, allowing for easier comparison with existing industry and academic data. Table 1 summarizes the SONY-MURATA VTC6 datasheet. The cell's datasheet also provides the OCV–SOC curve, which will be used as a reference to benchmark the test results discussed in the following sections.

V_{max}	4.2 V
V_{nom}	3.6 V
V_{min}	2.5 V
Nominal Capacity	3000 mAh
Max Continuous Discharge Current	15 A
Weight	46.7g
Chemistry	INR Li-NiMnCoO2 (NMC)

Table 1: SONY-MURATA US18650VTC6 3000 mAh cell specifications

3.1.1 Discharge curve

We will cycle the cells using the Galvanostatic Intermittent Titration Technique (GITT), combining the methodologies proposed by Liu et al. [6], tested by Soto et al. [28], and Barai et al [29]. The cells were discharged at constant current for a fixed SOC jump $\Delta SOC = 5\%$, followed by a relaxation period of 1 minute, where the voltage of the cell was allowed to reach steady state. Figure 22 shows the discharge curve at 1C-rate, where cells were discharged at constant current during 3-minute intervals followed by a minute relaxation period, repeating the process a total of 20 times (until fully discharged). Note that the current is given not for a cell, but rather the total current of 6 cells in parallel

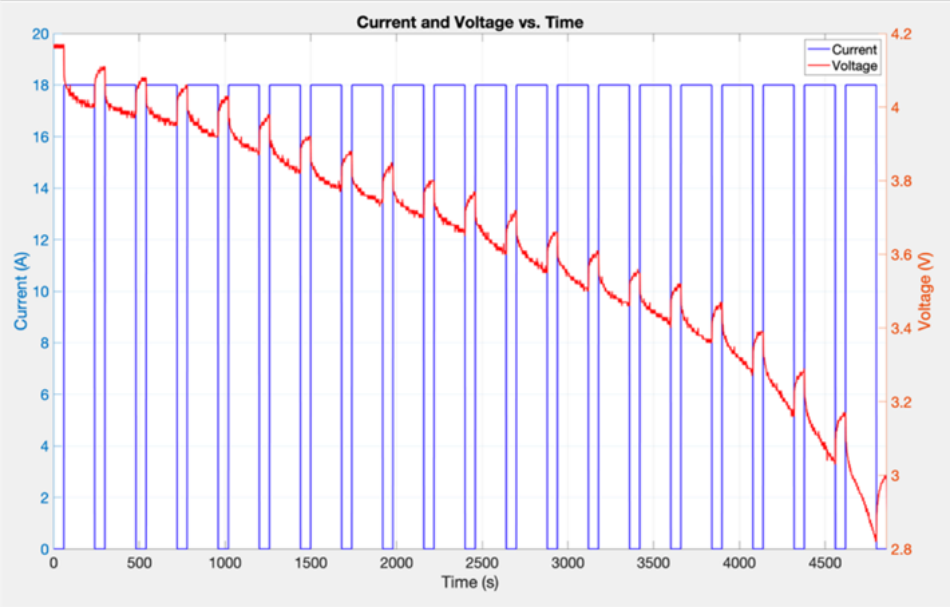


Figure 22: Current and Voltage vs Time for GITT cycle at 1C

The figure below, Figure 23 shows a close-up of the first two constant current pulses of Figure 22. The cells are initially discharged from max voltage (4.2V) and go through 20 continuous pulses, until the cell reaches the minimum terminal voltage. In between of each of the 20 pulses, the voltage is allowed to reach steady-state voltage during a relaxation period that last 60s.

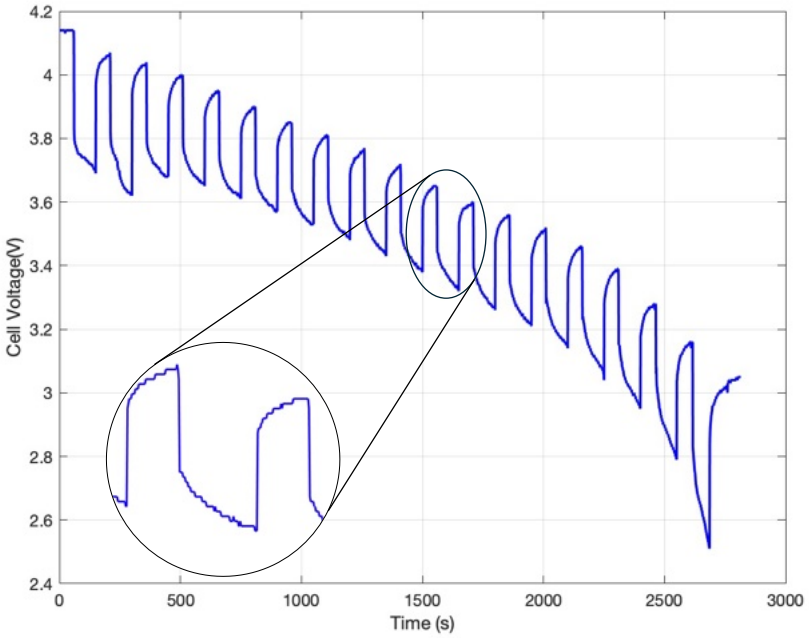


Figure 23: Close-up of GITT constant 1C current pulses and voltage vs time

To characterize both the 6x cell parallel and single cell models, they were discharged at the same C-rate pulse, using the GITT pulse pattern proposed by Liu et al. [6]. A total of three trials were repeated for every discharge curve for both the parallel and single cell configuration. For all the trials ΔSOC was fixed at 5%, so the pulse time was shortened accordingly to adjust for C-rate. The table below, Table 2, summarizes the discharge c-rate current, pulse length, relation period for all trials conducted with both the 6x cell parallel and single cell configuration:

Discharge C - Rate	Current Single Cell Configuration	Current Parallel Cell Configuration	Pulse length	Relaxation period
0.5C	1.5 A	9 A	360s	60s
1C	3 A	18 A	180s	60s
2C	6 A	36 A	90s	60s
3C	9 A	54 A	60s	60s

Table 2: Discharge curve list for both 6x cell parallel and single cell configuration

3.1.2 Control Variables

In addition to the pulse length and relaxation period, there were other critical parameters that were essential to control to ensure battery safety and enable reliable data comparison. The following table, Table 3, outlines how the variables are controlled in the test bank.

Control Variable	How is the variable controlled?
Initial SOC-Charging process	To maintain consistency in the initial state of charge (SOC) across all tests, we will charge each cell using the same procedure. The charging process of the cell has two stages. First, the cell is charged at a constant current of 500 mA. Once the cell reaches the maximum voltage, $V_{Max} = 4.2\,\text{V}$, it switches to constant voltage charging until the current drops below the minimum charge current, $I_{\text{Min}\,Charge} = 150\,mA$, which is 0.05C for VTC6 cells. All the cells will be charged using this charging procedure, discharging all the cells always from 100% charge.
Minimum Battery Terminal Voltage	Undervoltage can severely damage the battery, promoting dendrite formation and accelerating aging. To prevent this, the test bank will incorporate an undercharge safety mechanism in the code to ensure cells always operate within their safe voltage range. The discharge process will follow the GITT constant current pulse profile until the battery reaches the minimum terminal voltage, $V_{Min} = 2.5\,V$. Afterward, the battery will be disconnected from the load and allowed to reach a steady-state voltage.

Current	The GITT method requires to discharge the cell constant current rate. As the cell's voltage decreases with the state of charge (SOC), the resistive load must adjust accordingly to maintain a steady current. Given the high-power nature of the load, which requires drawing a high C-rate from the cells, an array of 17 parallel resistances and relays will be used to regulate the current. Although this will be discussed in more detail in a future section, the relays will open and close to adjust the variable load, allowing it to dissipate up to 54 A of constant current pulses.
Temperature	The cell temperatures were measured using DS18B20 digital temperature sensors. Three sensors were placed on each cell, and two additional sensors were used to monitor atmospheric thermal conditions, resulting in a total of 20 sensors for the six-cell parallel configuration. The cells were always subjected to natural convection conditions, with no fans or other active cooling methods used during the tests. The thermal boundary conditions were continuously monitored to ensure reliable data comparison, and mostly importantly control that the cell temperatures did not surpass T_{max} = 60. In the case that T>T_{max}, the test bank disconnected the cells from the load to prevent thermal runaway.

Table 3: Outline of the control variables and how they are measured

3.2 *Battery Test Banks*

As outlined in Sections 3.1.1 and 3.1.2, the batteries were tested using a GITT cycle, where the cell were discharged intermittently under a constant current load at different C-rates. Both GITT and HPPC cycles are fairly common tests and can be easily programmed into commercial battery cyclers. However, these devices can be expensive and difficult to obtain, for reference, a Chroma 19311-10 Battery Cell Tester costs around $25,000 [30]. Ultimately, cost and time were two major constraints when designing the experimental procedure to test the batteries. Therefore, it was decided that the best alternative was to build the battery test bank systems from the bottom up, using readily available power electronics and microcontrollers. There were a few challenges to address in the design. The first was creating a constant current load that remained regulated as the battery voltage dropped during the discharge cycle. Two alternative test bank designs were evaluated for the single-cell and parallel configurations: one employed a variable MOSFET load, while the other used relay-actuated shunt resistors. Figure 24: Single cell battery test bank setup below shows the single-cell test bank setup, where an Arduino Uno served as both the datalogger and the controller for the power electronics, as well as the cell shutdown and protection circuit. A power relay was used to disconnect and connect the cell to the load throughout the discharge cycle.

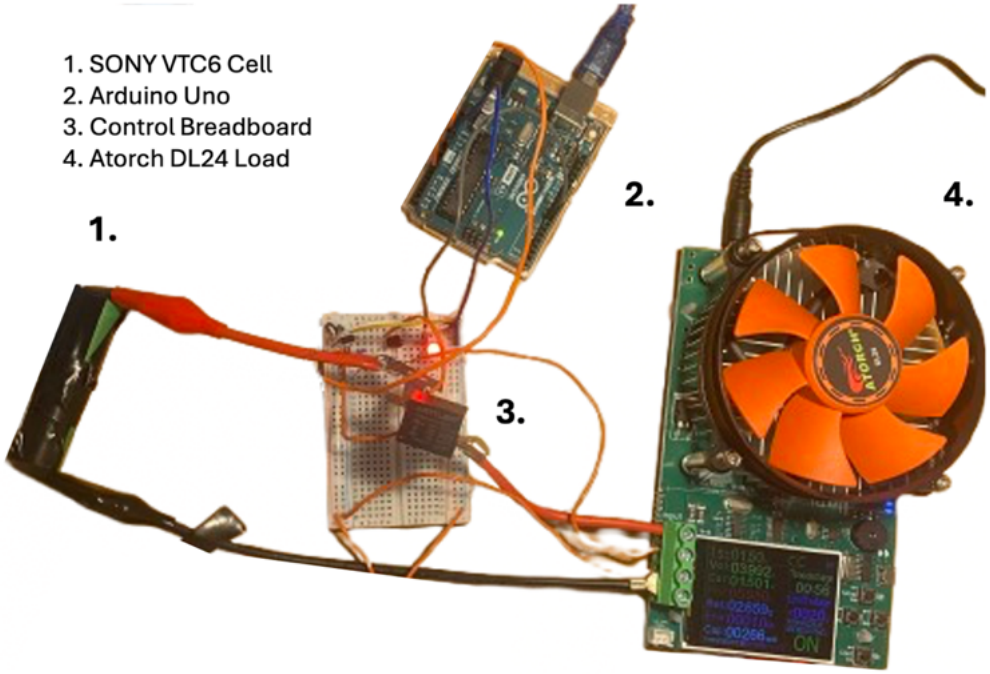


Figure 24: Single cell battery test bank setup

The single-cell test bank regulates discharge current with a maximum error of ±0.01 A. It supports discharge currents up to 20 A, with a peak power output of 180 W, sufficient for single-cell testing up to 6C. However, testing a six-cell parallel configuration under equivalent C-rate conditions requires discharging approximately 60 A, corresponding to six times the current and power. This demand necessitates a complete redesign of the load and power electronics to ensure safe and reliable operation under high-current conditions.

Figure 25 presents the six-cell parallel battery test bank. The system comprises three main components: the variable resistance load, the battery holder with copper bus bars, and an Arduino MEGA 2560, which functions as both the data logger and system controller. To accommodate the increased current, all conductive pathways are redesigned. In addition to supporting regulated currents up to 54 A (corresponding to a 3C rate for six VTC6 cells), the parallel-cell test bench introduces several key improvements over the single-cell version. These include the ability to measure temperature at three distinct locations on each cell (top, middle, and bottom), as well as ambient and resistor temperatures.

The higher current requirements also necessitate replacing the previous power relay with a TE Kilovac series contactor. While test conditions remain consistent with those used in the single-cell setup, the method of current regulation differs. Rather than employing a MOSFET-based variable load, the system uses a network of 17 resistors and 11 relays to create a variable resistance controlled in response to cell voltage. The following section provides a detailed overview of this system's design.

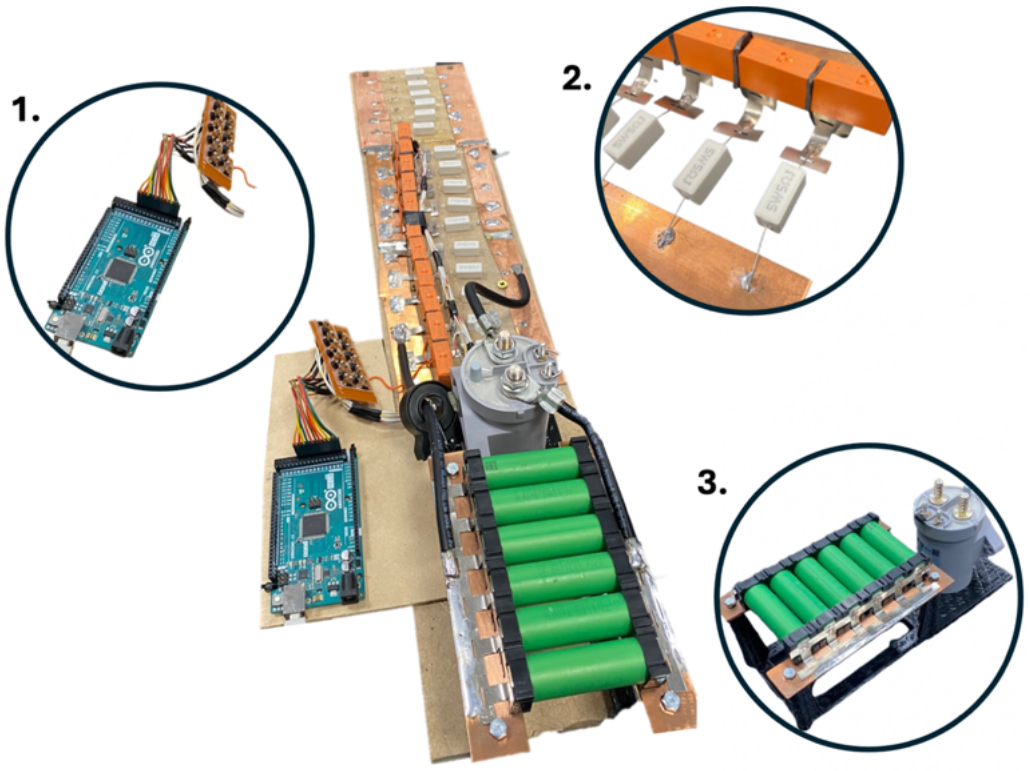


Figure 25: Cell parallel battery test bank setup

3.2.1 *Parallel Battery Test Bank Variable Impedance Load*

The design principle behind the variable impedance system is to provide a simple and accessible variable load capable of supporting high C-rate discharge pulses while maintaining a precise constant current throughout the discharge process. To achieve this, the design is reduced to its core: an array of parallel resistors. The primary challenge lies in determining the optimal number of parallel resistors, requiring an optimization of the resistance step size to ensure the current remains close to its setpoint while also allowing sufficient variability to compensate for large voltage drops. To sustain a 3C discharge rate across six parallel cells, the system must handle 54 A at 4.2 V, equivalent to 226.8 W.

The load consists of 17 parallel resistors. Six of these are large ceramic power resistors responsible for managing the majority of the current, while 11 smaller resistors are controlled via relays to enable fine current adjustments as the cell voltage decreases. Table 4 presents the different resistance configurations used for each discharge C-rate. It also includes the equivalent parallel resistance of the array as it transitions through various positions during the discharge. Positions 1 through 6 are fixed and are always connected during operation.

Position	Relay	$R_{0.5C}$	$R_{eq\ 0.5C}$	R_{1C}	$R_{eq\ 1C}$	R_{2C}	$R_{eq\ 2C}$	R_{3C}	$R_{eq\ 3C}$
1	No	5	5.00	1.5	1.50	1.5	1.50	0.5	0.50
2	No	5	2.50	1.5	0.75	1.5	0.75	0.5	0.25
3	No	5	1.67	1.5	0.50	1	0.43	0.5	0.17
4	No	5	1.25	1.5	0.38	0.5	0.23	0.5	0.13
5	No	5	1.00	1.5	0.30	0.5	0.16	0.5	0.10
6	No	5	0.83	1.5	0.25	0.5	0.12	0.5	0.08
7	Yes	5	0.71	5	0.24	2	0.11	1	0.08
8	Yes	5	0.63	5	0.23	2	0.11	1.5	0.07
9	Yes	5	0.56	5	0.22	2	0.10	1.5	0.07
10	Yes	5	0.50	5	0.21	2	0.10	1.5	0.07
11	Yes	5	0.45	5	0.20	2	0.09	1.5	0.06
12	Yes	5	0.42	5	0.19	2	0.09	1.5	0.06
13	Yes	5	0.38	5	0.19	2	0.08	1.5	0.06
14	Yes	5	0.36	5	0.18	2	0.08	1.5	0.06
15	Yes	5	0.33	5	0.17	2	0.08	1.5	0.05
16	Yes	5	0.31	5	0.17	2	0.08	1.5	0.05
17	Yes	5	0.29	5	0.16	2	0.07	1.5	0.05

Table 4: Resistance configuration (Ω) and equivalent parallel resistance R_{eq} (Ω) for 0.5C, 1C, 2C, 3C discharge rates rate

Using this configuration, the system achieves a variable resistance range from 5 Ω down to 51 mΩ, with a minimum step size of 1.7 mΩ for fine control, whilst capable of dissipating up to 520 W of power, more than sufficient for holding 3C discharge rate.

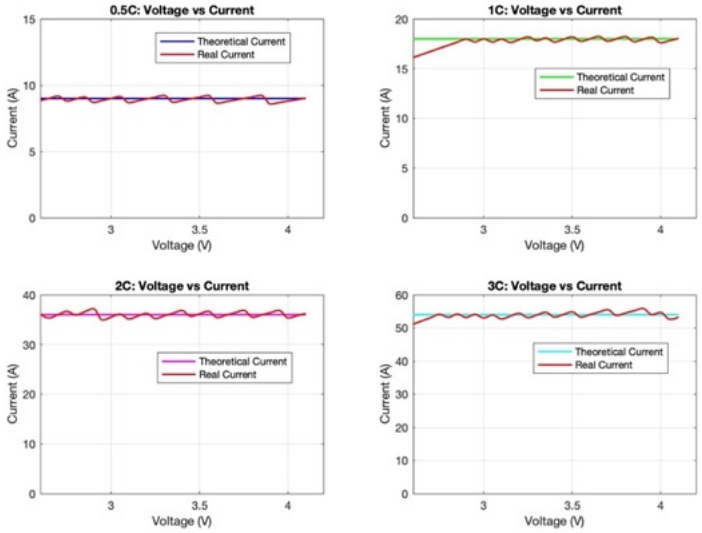


Figure 26: Theoretical current vs real current at different voltage for 0.5C,1C,2C,3C

Figure 26 and Figure 27 show real current passing through the load as the resistance changes with voltage at different discharge rates.

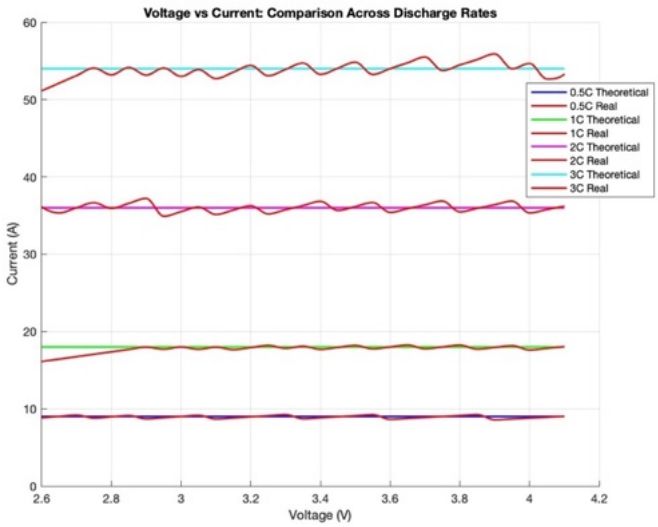


Figure 27: Theoretical current vs real current flow (A) through variable load at different battery voltage (V)

Although far from perfect, this first iteration of the test bank design allowed for cycling at currents upwards of 50A, a capability typically only found in industry-grade cyclers, which tend to be worth upwards of tens of thousands of euros. Even though the discrete nature of the variable load was a great and simple first approach to solving current regulation problem, it was not ideal, as it introduced significant transient currents when opening and closing the relays. This issue was considered when designing the following iterations of the test bank. Nevertheless, as seen in the following sections (reference data sections), the data was still very useful to determine cell behaviour at the parallel level. The figures below, Figure 28 and Figure 29 show the electrical schematics of the test bank, as well as a close-up of the relay actuator circuit for the switchable loads. In addition to the array 11 switchable and 6 fixed resistances, the test bank uses a TE KILOVAC LEV200 Series contactor [30], connect and disconnect the parallel from the load during the relaxation periods. Due to high holding current a step-up 12V relay is used to control the contactor winding current (see Figure 30) .

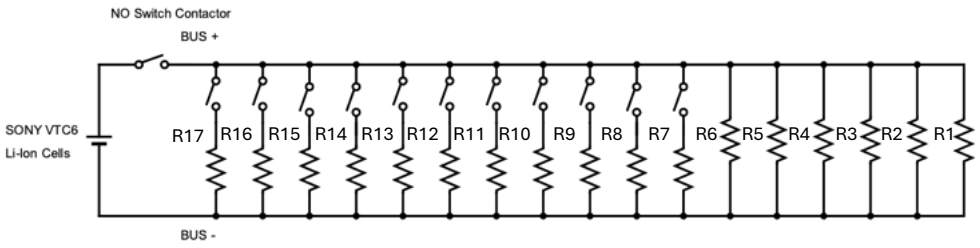


Figure 28: Battery Test V1 Electrical Schematics

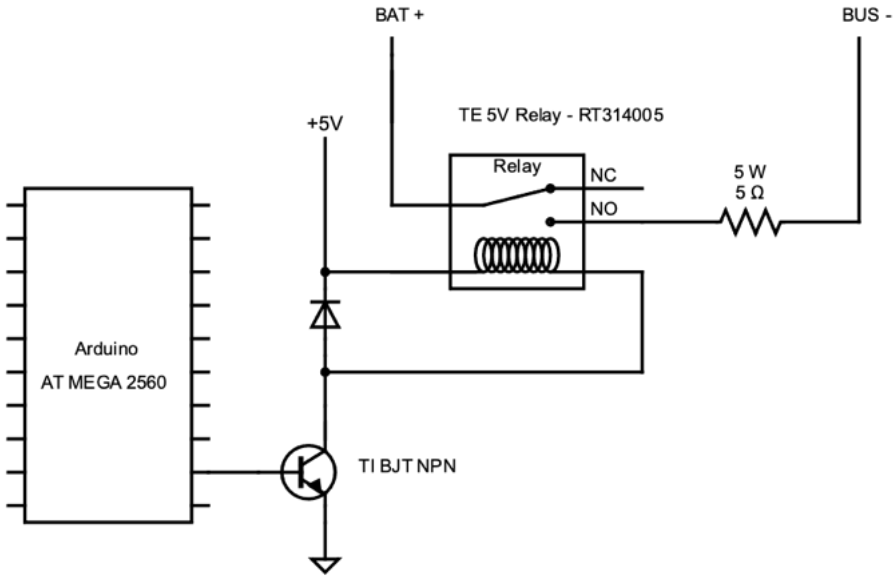


Figure 29: Parallel Battery Test Bank Relay Electrical Schematics

An Arduino ATMEGA 2560 was used to control the contactor (see Figure 30) and relays (see Figure 30Figure 29). It also functioned as a data logger for temperature and voltage, relaying all information to a PC used for storing and plotting the data in real time.

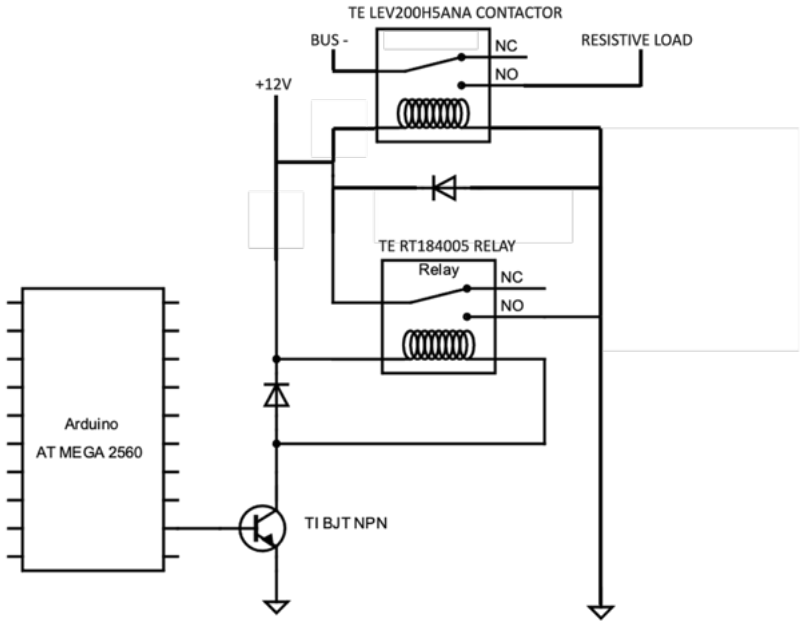


Figure 30: Parallel Battery Test Bank Contactor Control Circuit Schematics

3.2.2 *Temperature Sensors*

The internal resistance [31], the performance and safety of a battery cell [9] are completely dependent of the temperature of operation. Therefore, it is crucial to obtain accurate readings of both the cell temperature and the surrounding environment. The motivation behind designing the array of temperature sensors was to ensure that the test bank always operated within nominal conditions T<T_{max} = 60℃ and that any variations in ambient conditions could be tracked. Chen et al. [31] found that the cell temperature exhibited two noticeable gradients: one along the surface and another from the core to the surface. To measure the temperature of the core, Forgez et al. [9], proposed a method that inserted a nano-scale thermocouple into the center of the cell without significantly altering its chemical or mechanical properties. However, this method falls outside the scope of this study, as it requires extreme precision to install the thermocouple, something nearly impossible to achieve without specialized high-precision tools. The surface gradient, however, is much simpler to measure, requiring only three sensors to obtain a reliable estimate of the temperature slope. The Dallas DS18B20 digital temperature sensor was selected here, both for its small footprint and simplicity to use. A total of 20 sensors were used to monitor the cells and ambient temperature. As shown in Figure 31, Eighteen of them measured the temperature at the top, center, and bottom surfaces of each cell (three per cell for all six cells), while two additional sensors monitored the ambient temperature T_{inf} and the temperature of the resistive load T_{res}.

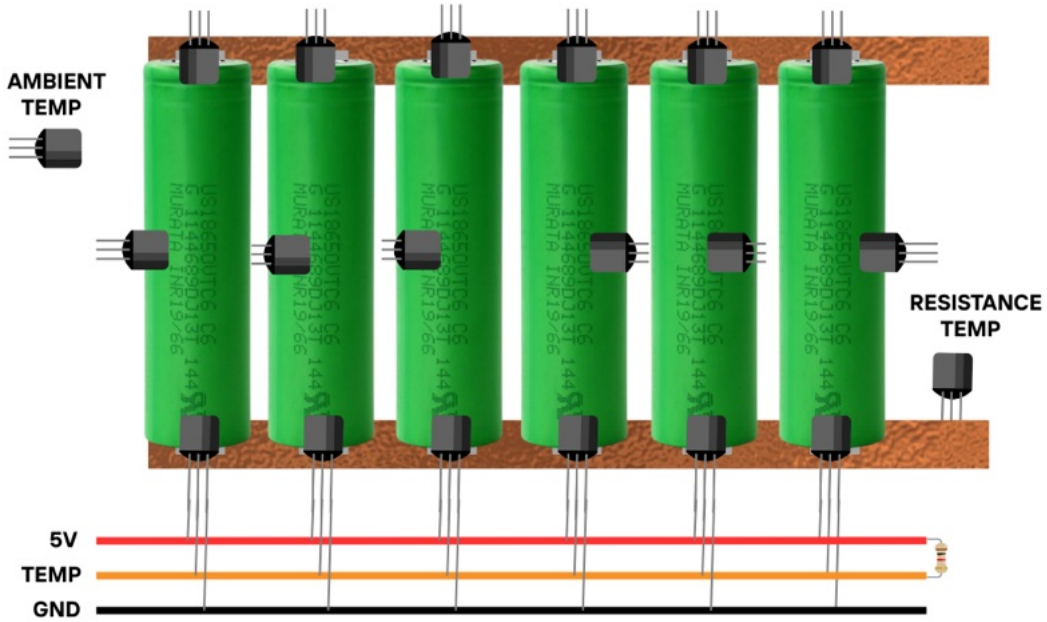


Figure 31: Dallas DS18B20 Temperature Sensor Array

3.2.3 *Battery Test Bank Control Logic*

As seen in Figure 32, at the start of any test, the ATMEGA 2560 microcontroller is initialized in the *Standby* state. Here, the ATMEGA 2560 searches for all 20 DS18B20 temperature sensors and the cell voltage readings, which have been previously assigned a sensor ID. If the board successfully reads all 20 temperature values and the cell voltage, and all measurements are within the operating range (below 60°C and with a voltage between 2.5V and 4.2V), the microcontroller transitions to the *Reading and Ready* state. The battery test bank then initializes the data logger, starts plotting data in MATLAB and records the signals on the local hard drive. After 60 seconds, the board moves to the *Discharge* state, closing the contactor. The test bank remains in this state under nominal conditions until the 5% SOC pulse ends, which lasts for 360 seconds at a 0.5C rate (see Figure 32). If at any point the cell voltage drops below 2.5V, the contactor opens to prevent cell damage, and the test bank transitions to the *Test Finish*ed state. Additionally, if during the discharge pulse any temperature reading is lost or any cell temperature exceeds 60°C, the test bank aborts the test and enters the *Emergency Stop* state. Under nominal conditions, once the discharge pulse is completed, the test bank enters the *Relaxation* state, where the contactor remains open for 60 seconds, allowing the battery voltage to reach steady state. Finally, if the test is completed under nominal conditions, the test bank transitions to the CC-CV *Charge* state, where the cells are charged using a CC-CV charging curve until their voltage reaches 4.2V and the charging current drops below 150mA.

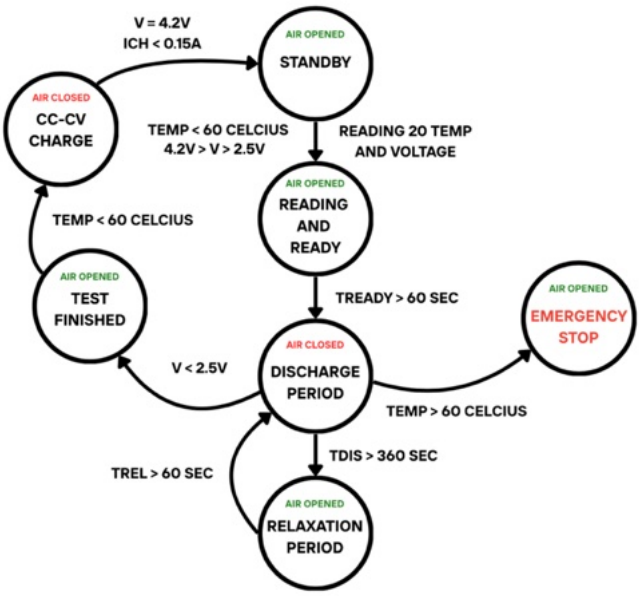


Figure 32: Test Bank AT 2560 Simplified State Machine Diagram

3.2.4 Short circuit destructive test design

The goal of this test was to better understand the mechanisms behind thermal runaway in cells, particularly when triggered by an external short circuit (ESC) (see Section 2.3.4). More specifically, the experiment aimed to investigate how the state of charge (SOC) influences both the reaction speed and peak temperature during thermal runaway (TR). Doose et al. [33] found a significant direct relationship between SOC and the peak temperature of TR, noting that thermal runaway did not occur at SOC levels below 30% [33]. Following the methodology for inducing ESC proposed by Bo Zhanga et al. [34], all cells were fully discharged to 2.5 V and then charged at 1C (3 A) until they reached the desired SOC. Table 5 shows the cell SOC levels before the ESC tests.

Trial	Short circuit @ SOC	Charging time (from 0% SOC)
1	0%	0 min
2	20%	12 min
3	60%	36 min
4	80%	48 min
5	90%	54 min
6	100%	60 min

Table 5: SOC of cells before External Short Circuit

Similarly to the setup proposed by Bo Zhang et al., a copper bus with a high-current manual toggle switch was used to externally short-circuit the cell [34]. The cells were connected to the copper bus bar under mechanical pressure to ensure they remained in contact even if the high temperature melted the solder connecting them to the DC bus. To monitor cell temperature, a DS18B20 metal-encapsulated digital temperature sensor was used. The sensor was placed at the center of the cell's side surface to capture the temperature closest to the cell's interior. After charging the cells from 0% SOC to the desired starting SOC at a 1C rate, the temperature probe was activated, and the manual switch was engaged from a safe distance. The experiment was conducted in a well-ventilated outdoor space. The battery cell was enclosed within a fire shield, and a 2-meter safety radius was established to prevent potential flames from igniting nearby objects in the event of thermal runaway. Once the cell was short-circuited, the test was allowed to run until the temperature dropped by 20 °C from the peak temperature or, in the case of thermal runaway, until it fell below the thermal runaway threshold (60 °C).

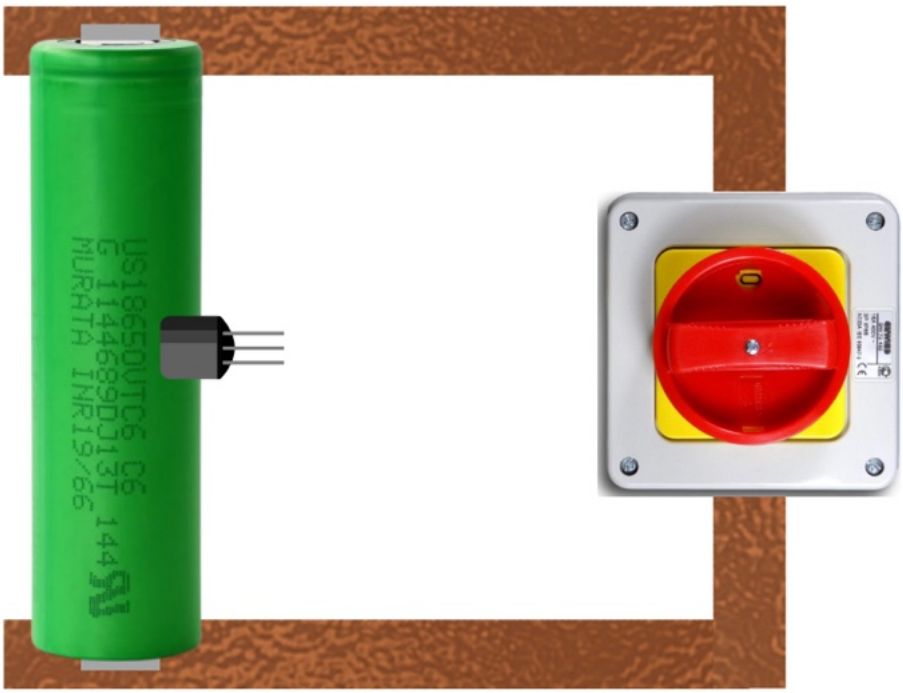


Figure 33: Cell thermal runaway test setup

The cells used in this test were SONY-MURATA VTC6 18650 cylindrical cells (3000 mAh), all with relatively similar states of health and lifecycles, having undergone approximately 15 full charge-discharge cycles prior to testing. They were stored and purchased at the same time to ensure consistency between cells. A camera was set up to monitor potential venting events. An ABC dry chemical extinguisher was kept nearby in case the fire extended beyond the containment area. Additionally, a water container was available for emergency use, and all short-circuited cells were submerged in it after testing for safe disposal and transport.

4. Battery Cycling Results

4.1 *Single Cell Galvanostatic Intermittent Titration Test*

Using the single-cell variable load test bank, the Sony-Murata 3Ah VTC6 cells were cycled at 0.5C, 1C, 2C, and 3C, or 1.5A, 3A, 6A, and 9A, respectively. As seen in Figure 34, the cell experiences an instantaneous voltage drop when current is drawn. This instantaneous drop is not constant throughout the entire discharge; it is more pronounced during the first two pulses and increases significantly toward the end of the discharge. This behavior suggests that the internal resistance of the cell is higher at both the beginning and the end of the discharge. After the initial voltage drop, the cell exhibits a transient voltage response. It is important to note that although a 60-second relaxation period captures most of the transient behavior, it is not sufficient for the cell voltage to reach a full steady state. In most cases, the voltage remained relatively stable toward the end, increasing by at most 0.01V over the last 10 seconds of the relaxation period. Nevertheless, the transient periods need to be extrapolated to determine the open-circuit voltage (OCV), resistance (R2), and capacitance (C). In future tests, one possible improvement could be extending the rest period to fully capture the transient response and steady state. However, due to practical constraints, achieving this was challenging in this work, with the longest test already taking 2 hours and 20 minutes to complete.

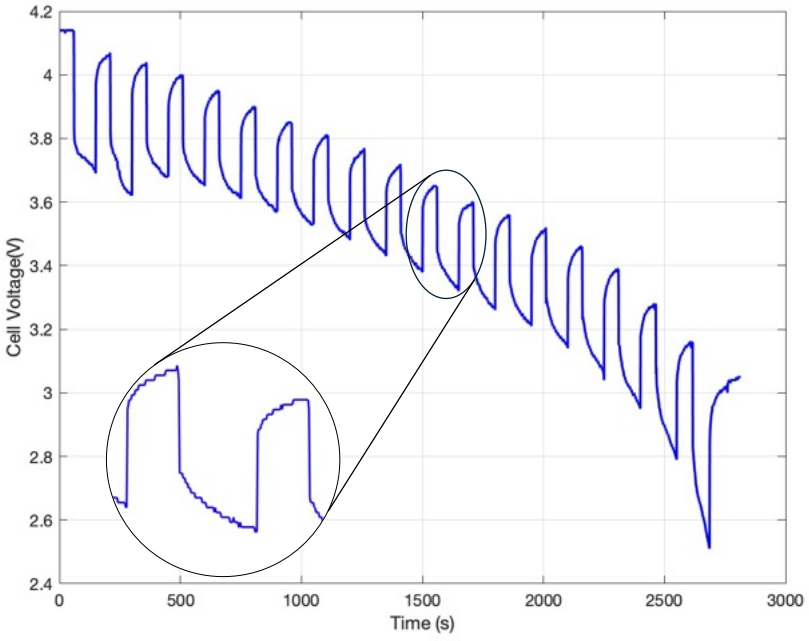


Figure 34: Cell Voltage (V) vs Time (s) Under 2C GITT Discharge Curve

4.1.1 *Open Cell Voltage (V) vs State of Charge (%)*

Figure 35 shows the Open Cell Voltage (V) vs State of Charge (%) profiles of the VTC6 cells across different C-Rates. Despite starting at the same initial voltage, even during the first disconnection period at 95% SOC, there are discrepancies between the OCV values of each trial (see Figure 35a and b). While most of these differences are minor across trials, trial 1C_3 exhibits a noticeable initial offset of approximately 0.05 V compared to the others. One possible source of this variation is the actual initial SOC. If the threshold current used to terminate the CC-CV charging phase was inaccurately measured in any of the trials, the resulting SOC could be higher or lower than expected, leading to a shifted OCV. Given that the approximate slope of the OCV–SOC curve between 95% and 40% SOC is around 0.01 V/%SOC, a 0.05 V offset could correspond to an SOC deviation of approximately 5%. Such an error could be critical if propagated into an electric vehicle's BMS.

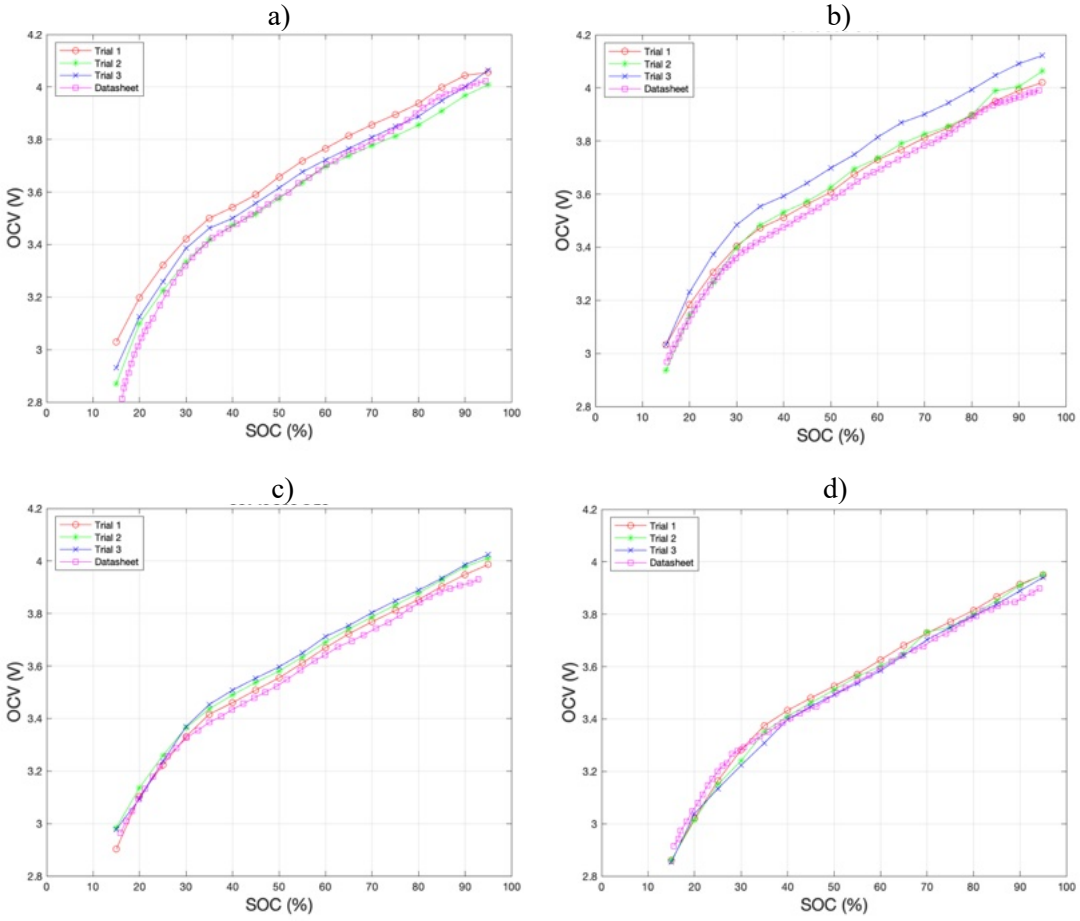


Figure 35: Open Circuit Voltage (V) vs. State of Charge (%) Profiles of VTC6 Cells During GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

While initial SOC offset is a plausible explanation, slight differences in electrochemical behavior between cells cannot be entirely ruled out. Another key observation from the single-cell test was that the cell discharged earlier than expected, indicating that the energy available at higher discharge rates was less than the total capacity of the cell. This is particularly interesting, as a general trend can be observed: at higher C-rates, less energy can be extracted during a full discharge. This can be observed in *Figure 35* c) and d), for the same SOC (%), the OCV at 3C is on average around 0.04V lower than the OCV at 2C, 0.1V lower than 1C, and 0.15V lower than 0.5C, which, for a constant current, results in less total energy being released.

4.1.2 *Internal Impedance R1 (Ω) vs State of Charge (%)*

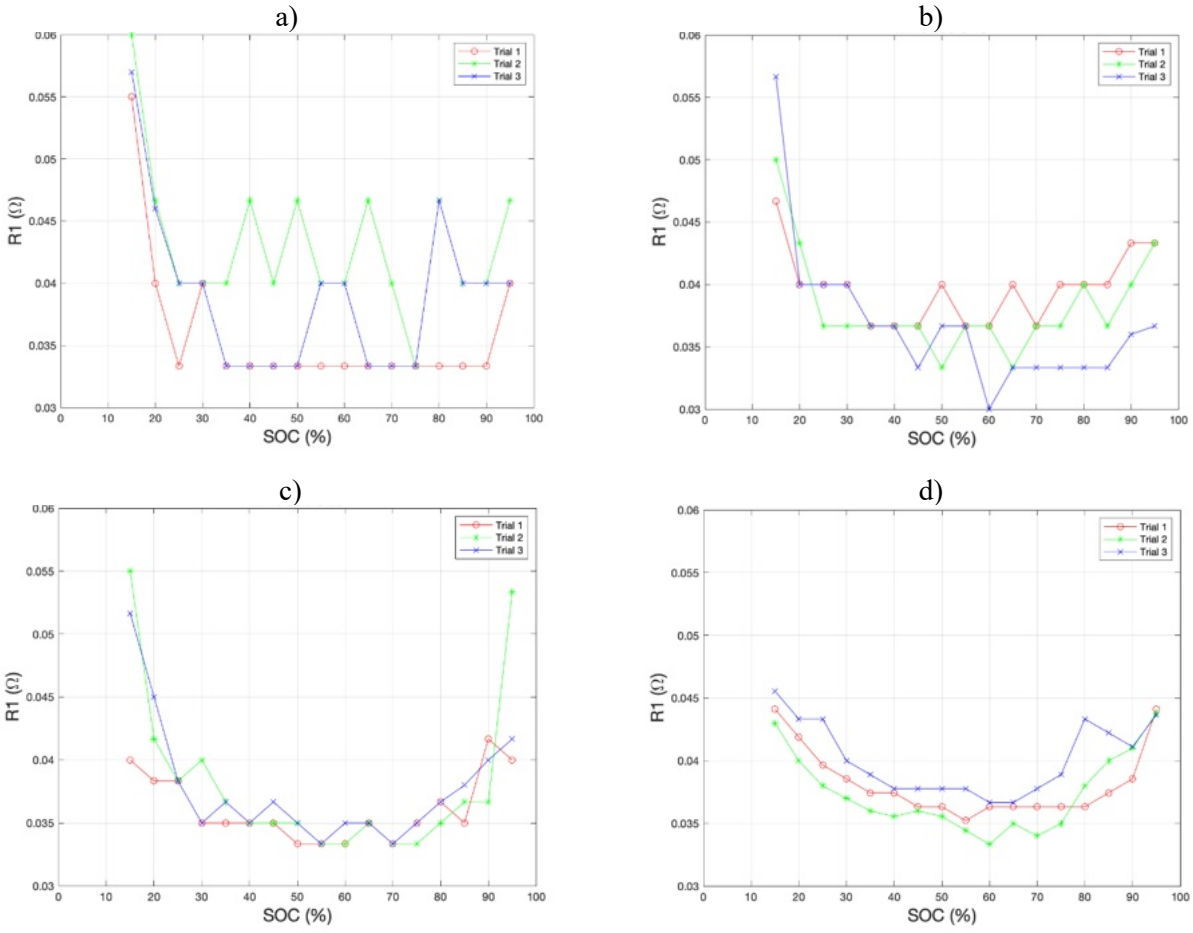


Figure 36: Internal Impedance R1 (Ω) vs. State of Charge (%) Profiles of VTC6 Cells During GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Using the instantaneous voltage drop, the internal impedance R1 was calculated. As expected from the observations in Figure 36, across all C-rates, the internal resistance R1 was higher at both the beginning and end of the discharge. This behavior is consistent with the underlying electrochemical processes: as lithium ions accumulate in the graphite anode, it becomes increasingly difficult for additional ions to intercalate into the structure, leading to a rise in resistance. This phenomenon is analogous to filling a bookshelf, when the shelves are nearly full, finding space for additional books becomes increasingly difficult.

Additionally, a few other interesting trends were observed. Although the results exhibit a clear U-shaped profile across all C-rates, some noise is particularly evident at lower C-rates. For instance, in trial 0.5C_2, the internal impedance fluctuates between 0.40 Ω and 0.47 Ω within the 70%–30% SOC range, suggesting a possible lack of resolution in the voltage measurement. This is especially noticeable at lower C-rates due to the smaller IR drop associated with lower currents, which makes the voltage measurements relatively less precise and more susceptible to noise.

For future tests, a potential improvement would be to use more precise voltage sensors. In this case, a 12-bit analog-to-digital converter was used, but in the future, it would be highly recommended to use a more precise digital multimeter connected to the data logger, which could increase the precision of the lower C-rate voltage drop measurements. Aside from the 0.5C test, another notable observation is the spike around 95% SOC in Figure 36c. This appears to result from an abnormal voltage drop, most likely caused by an incorrect voltage reading during the first few seconds after disconnection.

4.1.3 *Polarization impedance R2 (Ω) vs State of Charge (%)*

The R2 component reveals several interesting trends related to the transient behavior of the cells. As shown in Figure 37, a distinct U-shape appears across all discharge C-rates, indicating that the secondary polarization resistance is higher at both the beginning and end of the discharge cycle. At higher C-rates, the variation in R2 across SOC steps is less pronounced. In contrast, at 0.5C, there is a notable increase in internal resistance during the final disconnect, suggesting a slower transient response as the cell nears full discharge.

Using a similar analogy to the one applied to the internal impedance, as lithium ions accumulate in the anode structure, it becomes increasingly difficult for additional ions to intercalate, leading to a slower transient response. Once again, greater oscillation is observed at lower C-rates. At 0.5C, R2 fluctuates between 0.03 and 0.06 Ω in the middle

section of the discharge curve (80%–30% SOC), likely reflecting the limited resolution of the voltage measurement used to estimate transient behavior. Looking at the bigger picture, throughout all C-rate, the average value of the secondary polarization resistance remains within the range of 0.04 to 0.06 Ω throughout the central portion of the discharge (95%–35% SOC). However, to fully understand the cell's dynamic response, R2 must be considered in conjunction with the cell capacitance, as both parameters together determine the time constant and overall transient behavior.

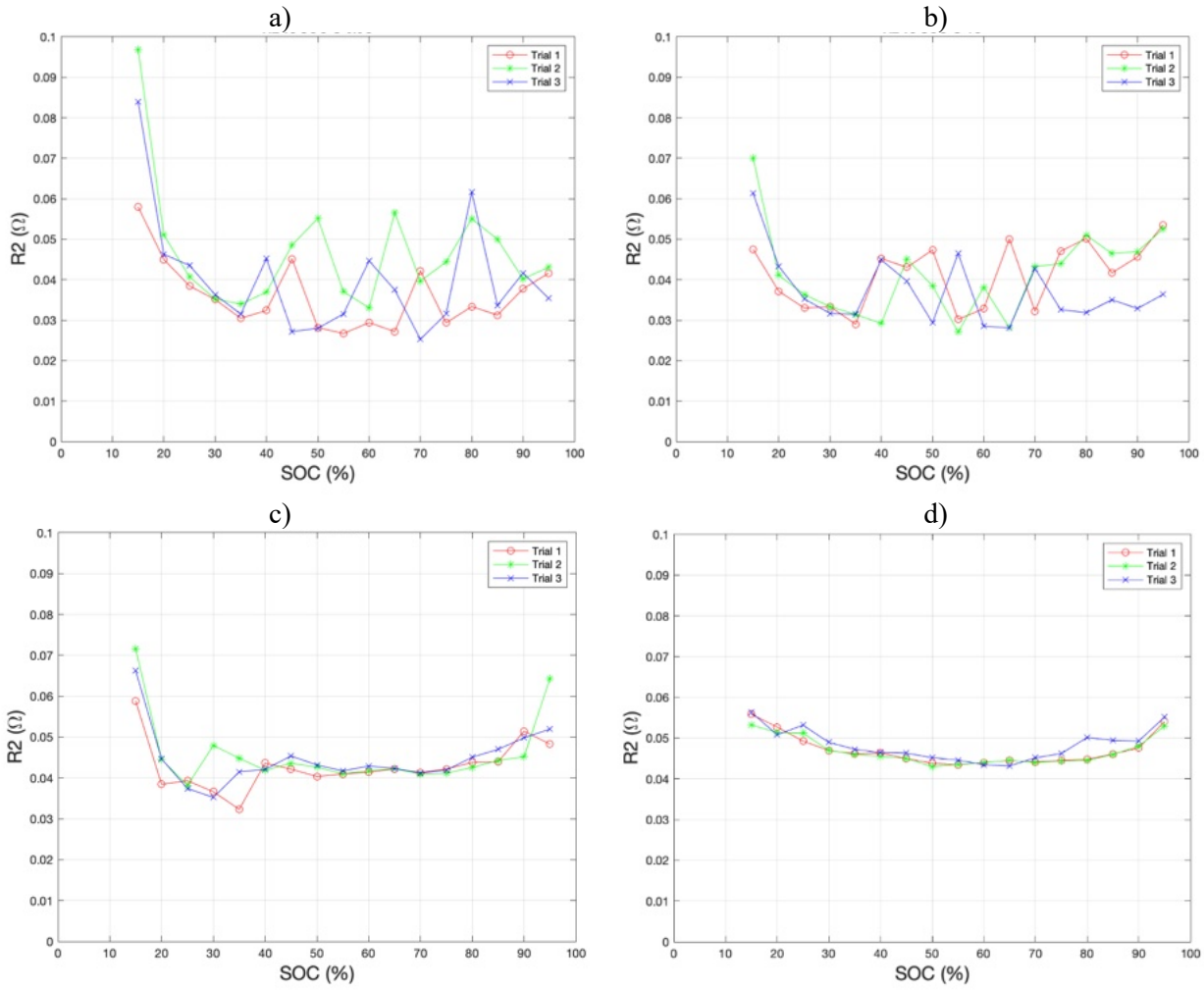


Figure 37: Internal Impedance R2 (Ω) vs. State of Charge (%) Profiles of VTC6 Cells During GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

4.1.4 *Internal capacitance C (F) vs State of Charge (%)*

Figure 38 reveals a clear trend: as the C-rate increases, the peak cell capacitance decreases. At 0.5C, the cell reaches a peak capacitance of 464 Farads at 35% SOC (Figure 38a), whereas at 3C, the peak drops dramatically to just 42 Farads—more than ten times lower. This suggests that the transient behavior of the cell when disconnected from the load is significantly faster at higher discharge rates. Another notable observation is the higher variability in capacitance between disconnects and trials at lower C-rates. It remains unclear whether this variability stems from intrinsic cell behavior or from measurement uncertainties, and further analysis is required to clarify this. Still, a consistent pattern emerges in Figure 38c and 38d, where capacitance peaks toward the end of discharge: around 15% SOC for 3C and between 40%–25% SOC for 2C. Overall, the data suggests that as C-rate increases, so does the speed of the cell's transient response after disconnected from a constant current step.

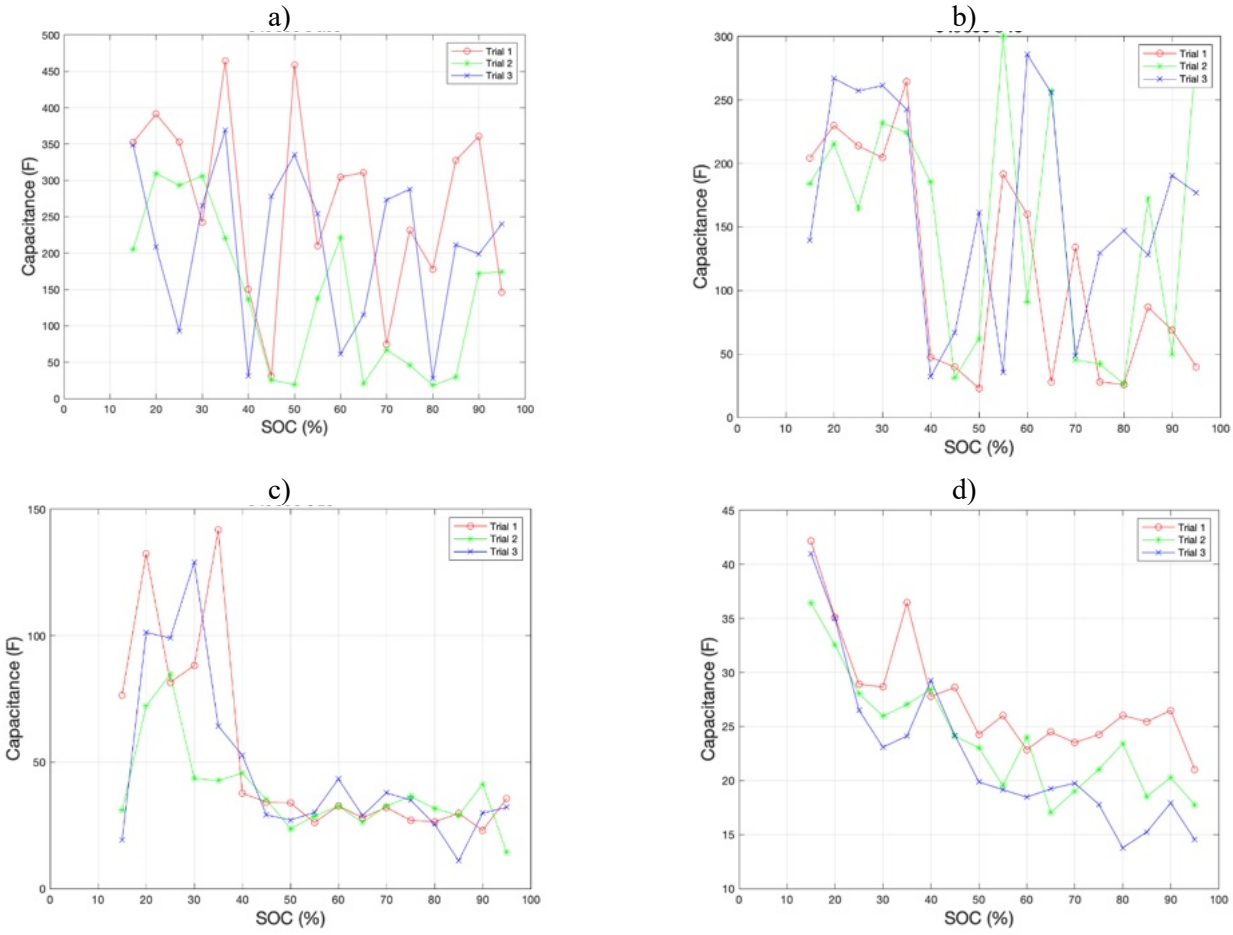


Figure 38: Cell Capacitance C (F) vs. State of Charge (%) Profiles of VTC6 Cells During GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

4.1.5 *Effect of C-rate on Open Cell Voltage (V)*

Figure 39 shows the average Open Circuit Voltage (V) versus State of Charge (%) for all three trials at 0.5C, 1.0C, 2.0C, and 3.0C. Several key trends can be extracted from the figure. Firstly, as the C-rate increases, the Open Circuit Voltage at a given SOC decrease. When this observation is extended to the area under the OCV curve, it suggests that lower C-rates enable greater energy extraction, since the voltage remains higher throughout most of the discharge:

$$\text{Total Energy} = \text{Q}_{\text{nom}} \cdot \text{Area} = Q_{nom} \cdot \int_{15\%}^{95\%} OCV(SOC)\, dSOC$$

It can be observed that lower discharge C-rates allow for more total energy to be extracted from the cell. Figure 39 illustrates a sharper drop in OCV once SOC drops beneath the 40% threshold. It's important to note that the current data only characterizes the OCV-SOC relationship between 95% and 15% SOC; future work should aim to capture the full range, including both the initial and final stages of discharge. Another trend visible in Figure 39 is that the voltage offset between C-rates remains relatively constant during the early and middle stages of discharge. However, as the SOC approaches the lower end of the range, the OCV curves begin to converge, indicating that the rate-dependent voltage differences diminish near the end of discharge.

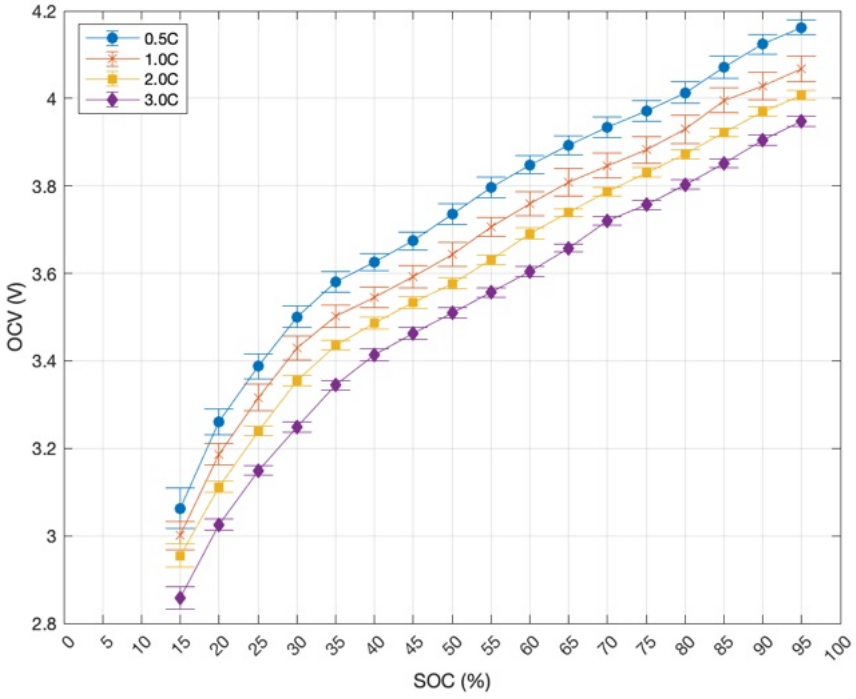


Figure 39: C-Rate Dependance of the OCV (V) vs SOC (%) Curve

4.1.6 *Effect of C-rate on internal impedance R1 (Ω)*

Figure 40 compares the average internal impedance R1 (Ω) versus State of Charge (SOC) across all C-rates. The data shows a consistent trend: for all C-rates, internal impedance increases at both the beginning and end of the discharge cycle. This behavior can be explained by examining the mechanisms driving internal resistance. At the start of discharge, when the cell is fully charged, most lithium-ions are intercalated in the anode. This tightly packed configuration makes it harder for ions to de-intercalate and begin migrating to the cathode, resulting in higher initial resistance. Once the SOC drops below approximately 80%, the lithium-ions begin to flow more freely, leading to a decrease in internal impedance during the mid-phase of the discharge. As the battery nears the end of discharge, resistance increases again.

This is due to lithium-ion accumulation in the cathode's graphite structure, making it increasingly difficult for additional ions to intercalate. It's analogous to a crowded library shelf, the more books already shelved, the harder it becomes to fit in a new one or take one out. Interestingly, among all C-rates, 1C shows the highest internal resistance peak, reaching 0.0511 Ω at 15% SOC. Consistent with trends observed in previous figures, variation between SOC steps decreases as the C-rate increases, indicating more stable behavior under higher current loads.

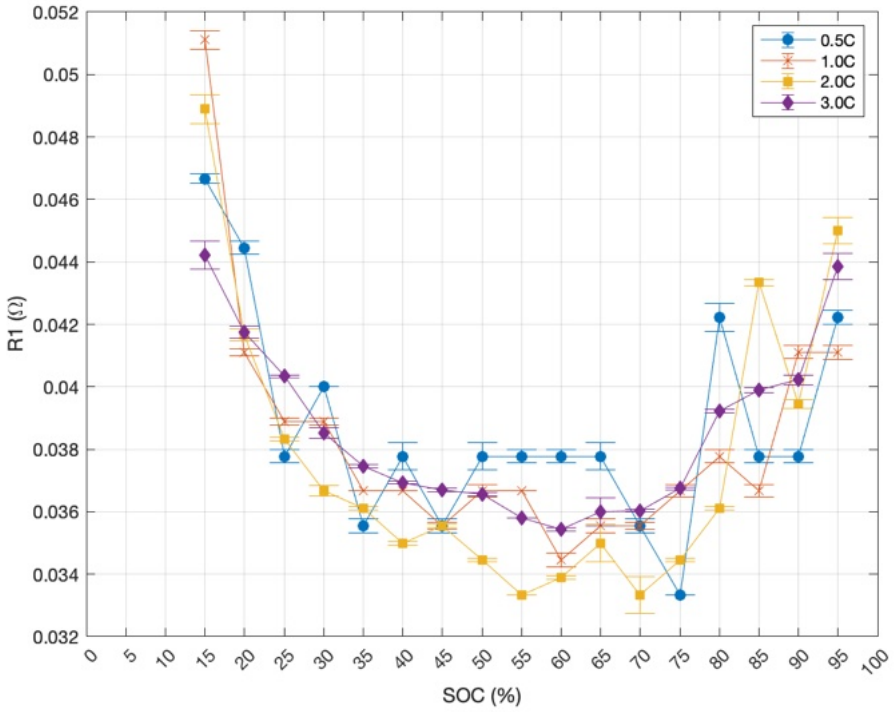


Figure 40: C-Rate Dependance of the Internal Impedance R1 (Ω) vs SOC (%) Curve

4.1.7 *Effect of C-rate on cell transient response*

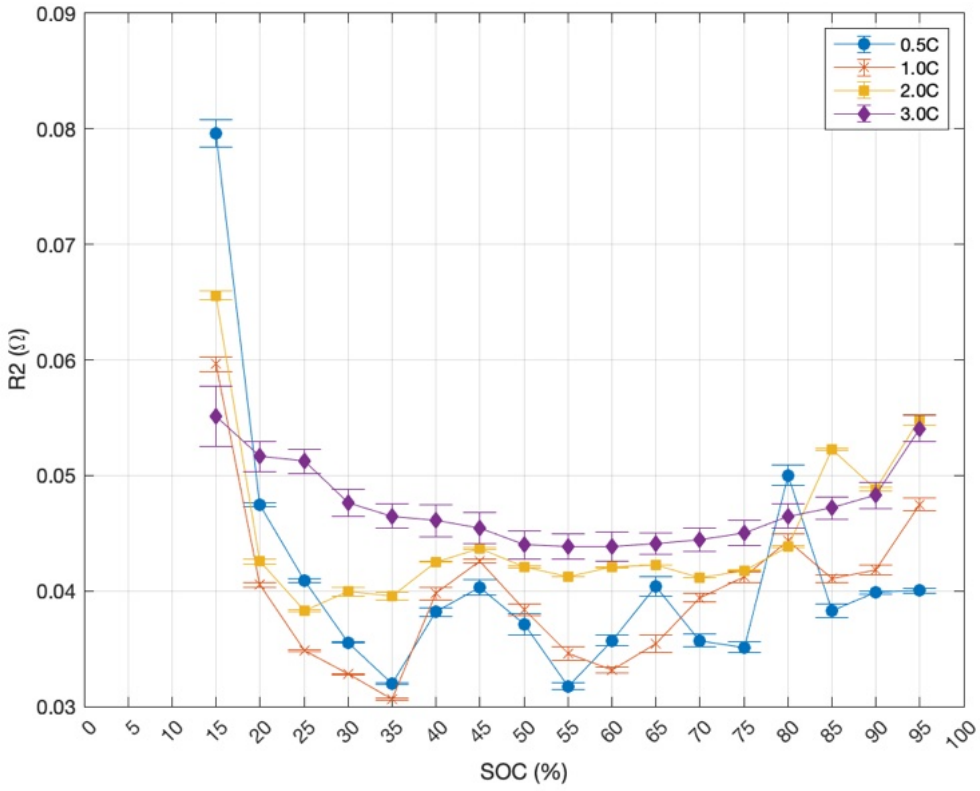


Figure 41: C-Rate Dependance of the Internal Impedance R2 (Ω) vs SOC (%) Curve

Figure 41, compares the average secondary cell impedance against SOC, throughout the four the discharge C-rates. Similar to internal impedance R1(Ω), which indicates the immediate polarization resistance of the cell, the trends observed in the figure above, indicate the secondary resistance across all the C-rates peaks at the end of the discharge. This peak is again, most significant for 0.5C, 1C and 2C with a relatively smaller peak for 3C. Overall this indicates that as the battery is discharged the transient behavior of the cell slows down in the end, which ultimately means it takes more time to reach its steady state Open Cell Voltage.

Interestingly both 1C and 0.5C, experience smaller secondary peaks at around 45%, 80% SOC, with 0.5C experiencing a third one at 65% SOC. This could potentially indicate, the presence of other electrochemical behaviors that are altering the speed of the transient response of the battery, although to confirm this we would need to have a deeper look into the chemistry behind the Sony VTC6 18650. But beyond secondary cell impedance, C-rate has also a significant effect on the cell capacitance. The following figure, Figure 42, compares the capacitance of the cell across all the discharge curves. Both 1C, 0.5C experience similar peaks and valleys, throughout all the SOC range, particularly, peaks

at 35% and 55%-50% of SOC and local minimums at 25%, 40-45% and 80%, indicating a potentially more complex underlying electrochemical relationship between SOC (%) and capacitance. In Figure 42, it can also be clearly observed that generally capacitance is lower for larger C-rates, which was expected, as with higher C-rate a faster voltage transient was observed. For 2C and 3C a maximum was observed in the 15%-30% SOC region.

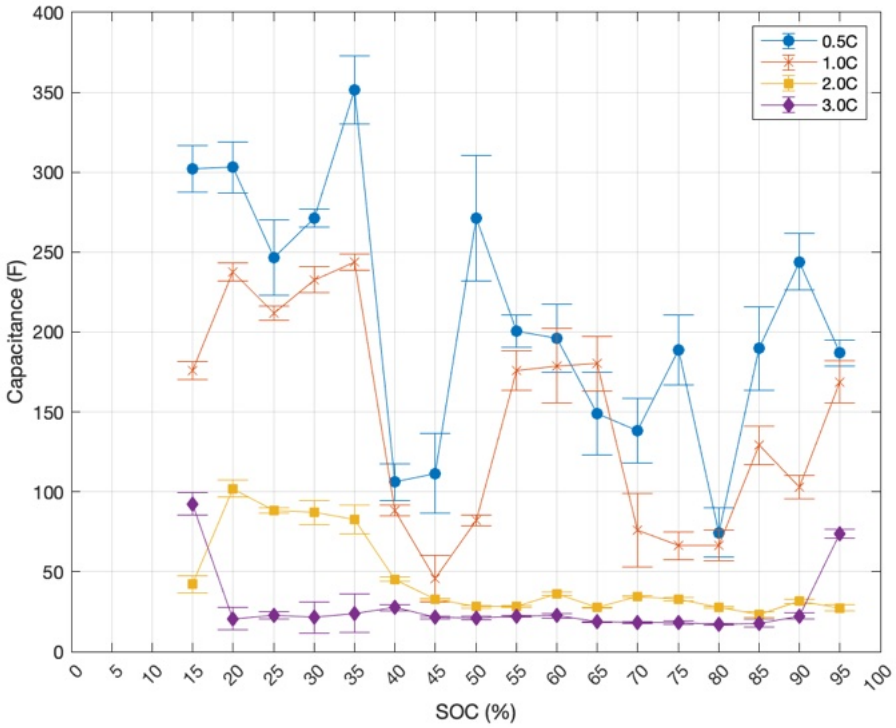


Figure 42: C-Rate Dependance of the Cell Capacitance (F) vs SOC (%) Curve

4.2 *6 Cell Parallel Galvanostatic Intermittent Titration Test*

Using the parallel variable load test bank (see Figure 25), six Sony-Murata 3Ah VTC6 cells were cycled following a GITT discharge profile at 0.5C, 1C, 2C, and 3C (corresponding to 9A, 18A, 36A, and 54A, respectively). Three trials were conducted for each C-rate. After each discharge, the cells were allowed to rest until they reached steady state before being recharged using a CC-CV protocol, continuing until the minimum charge current threshold was met. Figure 43 shows the voltage of the parallel under a 2C GITT discharge. As in the single-cell test, the voltage profile exhibits an instantaneous step at each connection and disconnection point, followed by a transient response that settles into a steady-state value. Notably, the slope of the terminal voltage under load increases significantly as the discharge progresses. Initially, during the first 2500 s, the

voltage declines at a rate of approximately 0.03 V/min. However, around 2750 s, this rate increases sharply, reaching approximately 0.41 V/min. This rapid change in slope indicates that once the terminal voltage approaches 3.0 V, continued discharge at 2C could cause the voltage to fall below the minimum operating limit (2.5 V) within about one minute. As such, accurate SOC estimation becomes critical near the end of discharge, where small changes in SOC can result in large voltage drops.

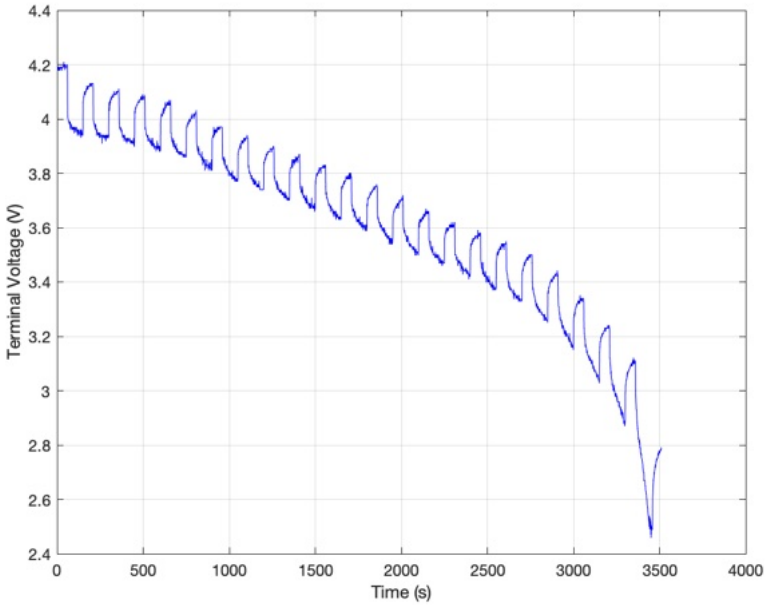


Figure 43: Parallel Cell Voltage (V) vs Time (s) Under 2C GITT Discharge Curve

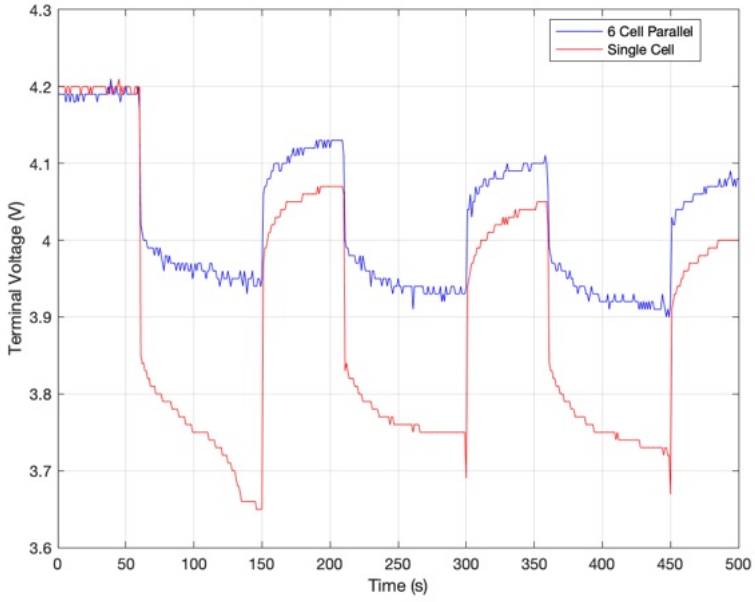


Figure 44: Close-Up of Parallel and Single-Cell Voltage (V) vs. Time (s) During 2C GITT Discharge

Figure 44 presents a comparison of the transient voltage response between a single cell and a six-cell parallel stack under the same C-rate. The parallel configuration exhibits a significantly smaller instantaneous voltage jump. At 95% SOC (the first disconnection), the voltage step for the parallel stack is approximately 0.12 V, compared to 0.32 V for the single cell. Notably, the single-cell profile shows a brief voltage drop immediately prior to disconnection, which increases the apparent step change. This may be attributed to noise introduced by the power electronics responsible for controlling disconnections and maintaining constant current. A more detailed comparison of the scaled-down resistances, presented in a subsequent section, will help clarify the effect of these differences on the calculated instantaneous resistance.

4.2.1 *Parallel Open Cell Voltage (V) vs State of Charge (%)*

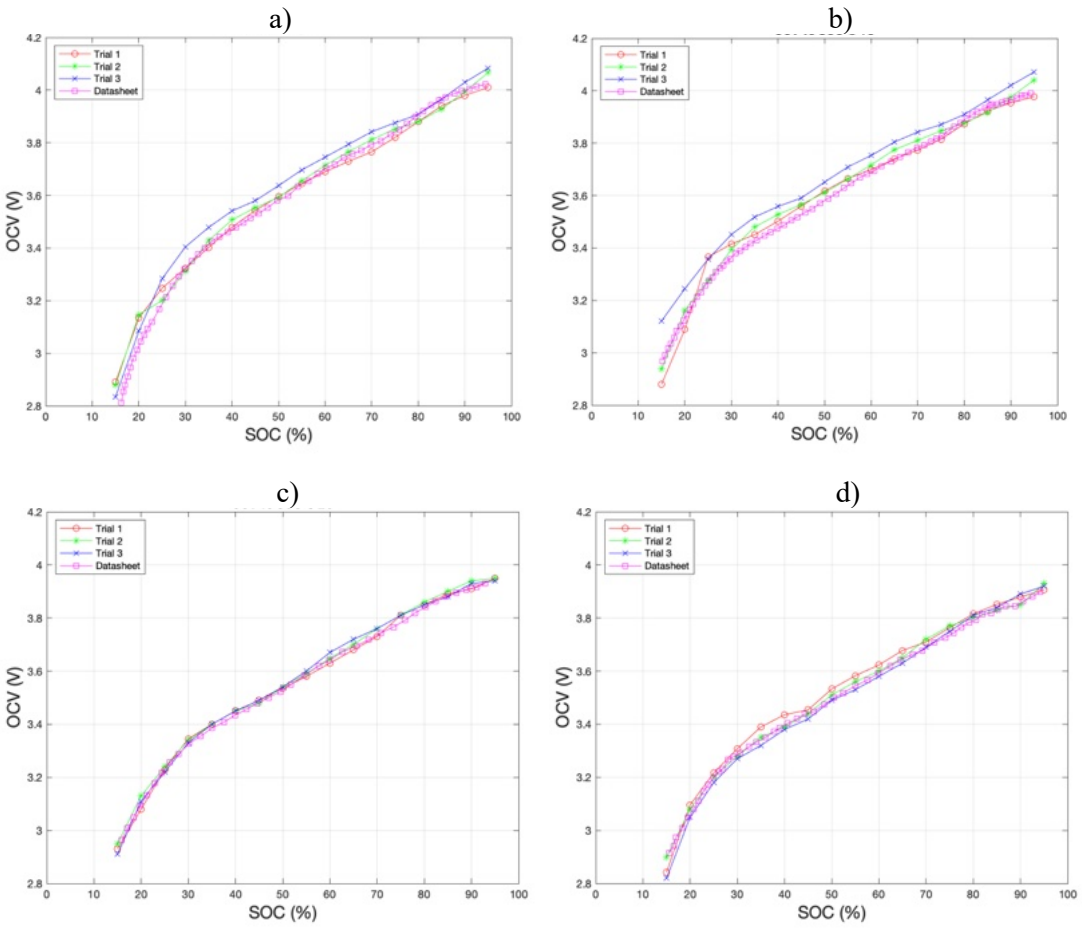


Figure 45: OCV (V) vs. SOC (%) Profiles of 6 VTC6 Cells in Parallel During under a GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Figure 45 presents the open circuit voltage (OCV) versus state of charge (SOC) profiles for a stack of six Sony VTC6 cells connected in parallel during GITT discharge tests at four different C-rates. Across all C-rates, the OCV–SOC curve exhibits a relatively consistent slope between 90% and 40% SOC, ranging from approximately 0.01 V/% to 0.015 V/%. Below 40% SOC, the slope increases significantly, approximately doubling to 0.02–0.03 V/%. Similar to observations from the single-cell tests, several trials, specifically trials 2 and 3 at 0.5C and 1C, show visible voltage offsets at the beginning of the discharge. These deviations may suggest an initial SOC mismatch, possibly due to incorrect charge termination, or inherent variation in the electrochemical properties of the cells. In addition, greater variability is observed at lower C-rates when compared to the manufacturer's datasheet, with trial 3 diverging by as much as 0.05 V from the datasheet expected value. Finally, trial 1 at 3C exhibits a distinct double hump in the OCV–SOC profile, with two local peaks and a valley centered around 45% SOC. This anomaly may be the result of a misreading during the corresponding rest period, as it doesn't not follow the general trend for the rest of discharge curves.

4.2.2 *Parallel internal impedance R1 (Ω) vs State of Charge (%)*

Stacking cell in parallel decreases the size of the instantaneous voltage drop underload, as previously observed in Figure 43 and Figure 44. This makes complete sense, as by adding them in parallel the equivalent resistance is given by:

$$\frac{1}{R_{eq_{par}}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_6}$$

Assuming that the impedance of the cells is the similar (which could be the case if all the cells have a similar State of Health):

$$\frac{1}{R_{eq_{par}}} = \frac{1}{R_{cell}} + \frac{1}{R_{cell}} + \frac{1}{R_{cell}} + \frac{1}{R_{cell}} + \frac{1}{R_{cell}} + \frac{1}{R_{cell}} = \frac{6}{R_{cell}}$$

$$R_{eq_{par}} = \frac{R_{cell}}{6}$$

The equivalent instantaneous impedance of the parallel stack is theoretically expected to be six times lower than that of a single cell. As shown in Figure 46a, the peak internal impedance at 0.5C for trials 1–3 ranges between 0.01–0.015 Ω and occurs at the end of the discharge, similar to the behavior observed in the single-cell test. In the single cell test, the peak resistance measured was 0.06 Ω, which is consistent with the expected scaling. However, not all resistance values align perfectly with the theoretical equivalent.

In Section 4.3, the parallel test parameters will be downscaled to a single-cell scale to enable a more detailed analysis of the similarities and discrepancies the cell dynamics.

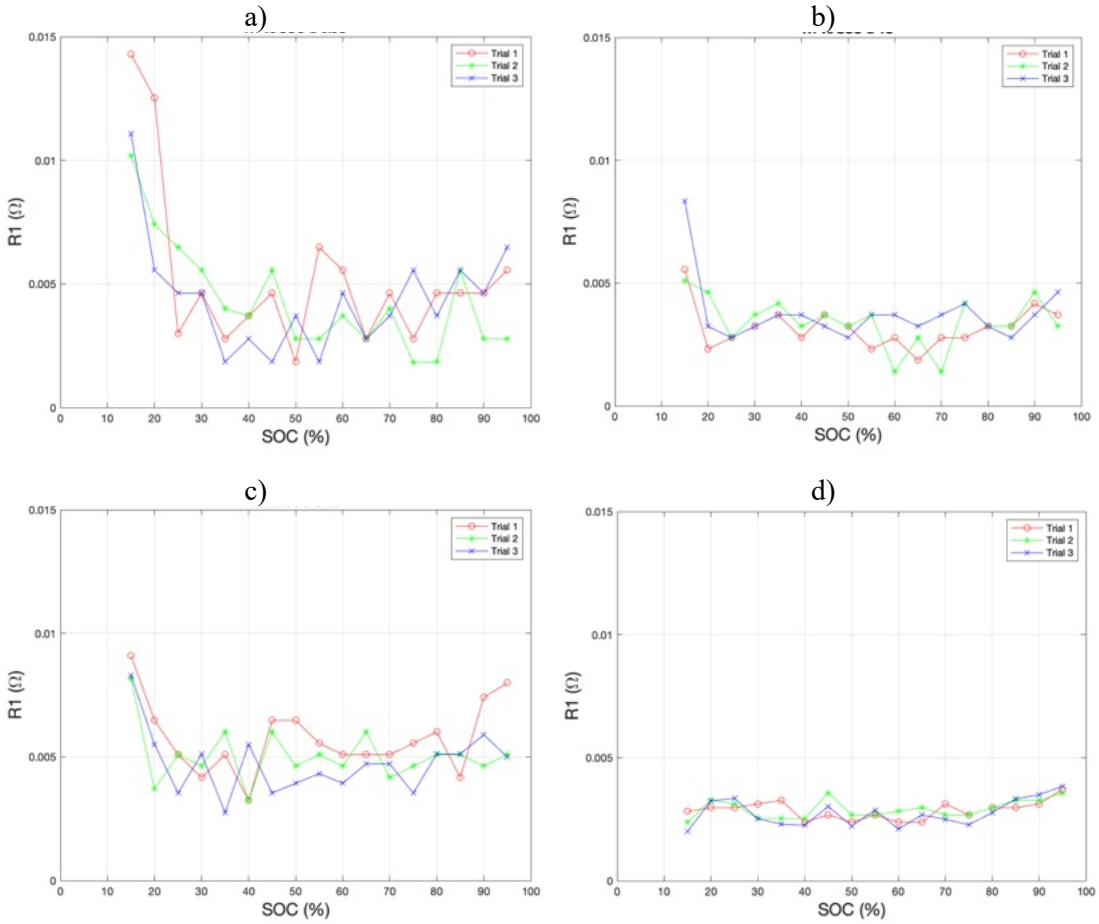


Figure 46: Internal Impedance R1 (Ω) vs. State of Charge (%) Profiles of 6 VTC6 Cells in Parallel under a GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Interestingly, aside from a few outlier peaks, there is no clear evidence of increased internal impedance at the beginning of the discharge, a characteristic that is clearly observed in the single-cell results. Additionally, between 95% and 30% SOC, the internal impedance of the cell remains, on average, within the range of 0.002 Ω to 0.006 Ω. Significant oscillation is again observed at lower C-rates, reinforcing the need for higher-resolution voltage sensing to accurately capture the smaller voltage drops. Although a significant peak appears at the end of the 0.5C discharge, this peak becomes notably smaller at 1C and 2C and is virtually absent at 3C. This raises questions about the significance of internal impedance at higher C-rates and whether the final measurements are sufficiently precise. Future studies could explore the resistance behavior at very low SOC levels (e.g., 0%, 5%, and 15%) using shorter, narrower current pulses to better assess whether internal resistance increases consistently at the end of the discharge across all C-rates.

4.2.3 *Parallel internal impedance R2 (Ω) vs State of Charge (%)*

Figure 47 presents the variation of internal impedance R2 (Ω) as a function of State of Charge (%) across different C-rates for the parallel stack. At lower C-rates (0.5C and 1C), a significant peak is observed at 15% SOC, with R rising to approximately 0.016 Ω for 0.5C and 0.0065 Ω for 1C, indicating a pronounced slowdown in the transient response as the battery approaches full discharge. This behavior is consistent with the trends observed in the single-cell tests. In contrast, at higher C-rates (2C and 3C), no such peak is evident, aligning with the previously noted trends in R1 for the same C-rate. The overall trend suggests that higher C-rates result in lower R2 values, indicating faster transient responses. At 40% SOC and above, the average R2 stabilizes around 0.004 Ω for 0.5C, decreases to approximately 0.0025 Ω for 1C, and remains steady at about 0.002 Ω for both 2C and 3C. It is also noteworthy that at 1C, a secondary peak appears around the 50%–60% SOC range, possibly indicating more complex underlying electrochemical behavior at intermediate states of charge.

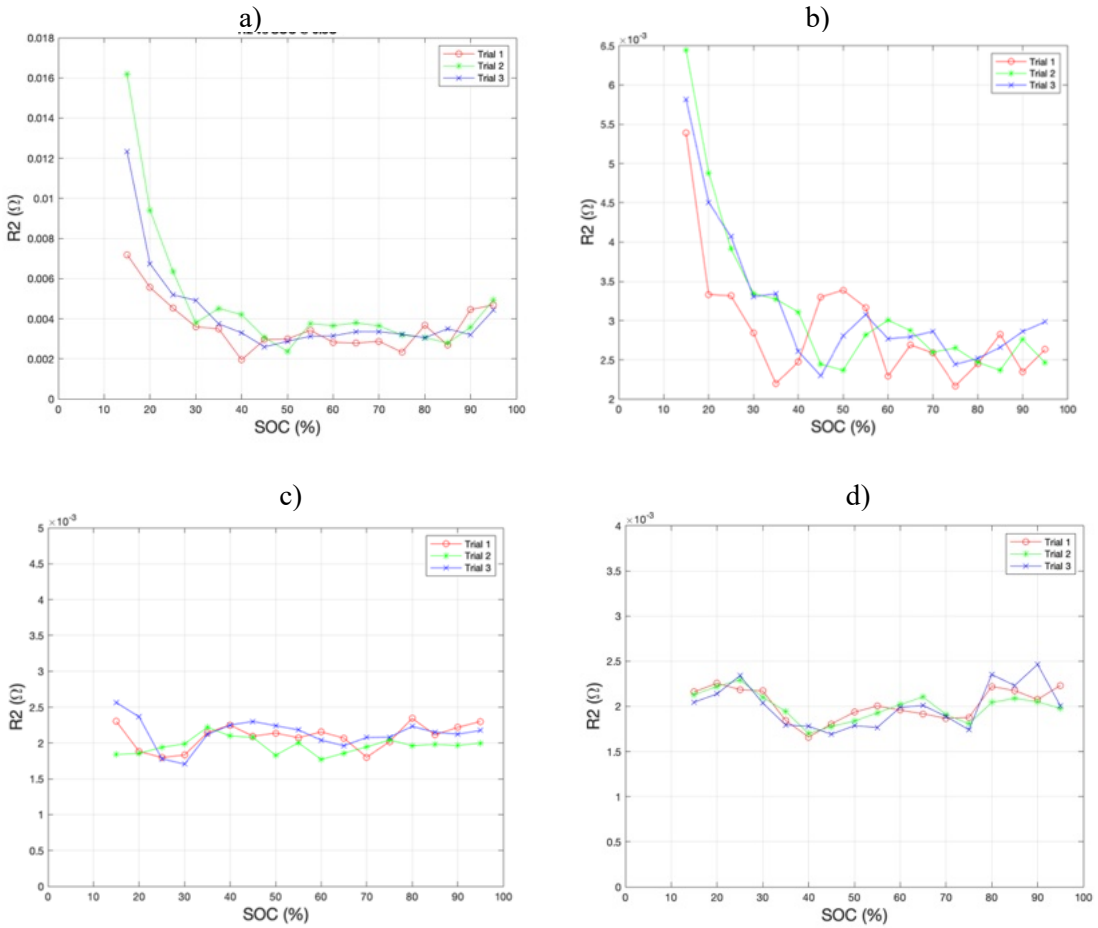


Figure 47: R2 Impedance (Ω) vs. State of Charge (%) Profiles of 6 VTC6 Cells in Parallel under a GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

4.2.4 *Parallel cell stack Capacitance (F) vs State of Charge (%)*

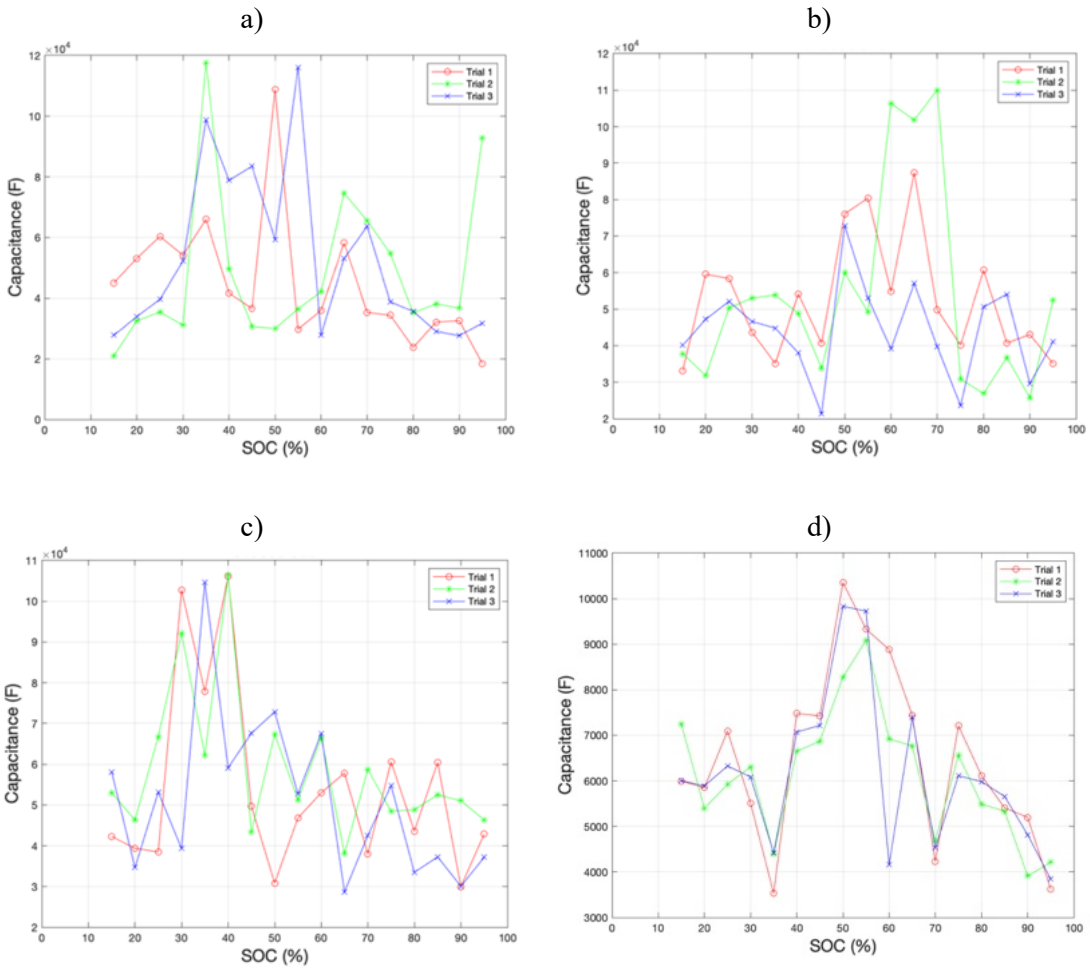


Figure 48: Capacitance (F) vs. State of Charge (%) Profiles of 6 VTC6 Cells in Parallel under a GITT Discharge at Different C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Figure 48 illustrates how the parallel stack's capacitance varies with state of charge (SOC) across different discharge rates. Despite noticeable oscillations in the data, particularly at lower C-rates, the overall capacitance of the parallel configuration appears significantly higher than that observed for a single cell. In general, the capacitance profile exhibits a peak approximately at the midpoint of the discharge curve. At 0.5C, capacitance peaks occur at 30%, 50%, and 55% SOC depending on the trial, reaching values around 12,0000 F. For 1C, the peak shifts earlier in the discharge, occurring near 70% SOC. At higher rates, the peak capacitance is observed around 30–40% SOC for 2C and near 50% for 3C. While the exact SOC at which the capacitance peaks vary, the peak values themselves are relatively consistent across all C-rates, around 11,0000-12,0000 F. Across the full SOC range, values generally decrease to around 30,000 F outside the peak region. Interestingly,

the capacitance values measured for the parallel stack are approximately 100–1000 times higher than those found in the single-cell tests. This raises important considerations for modeling transient behavior: rather than relying on both capacitance and R2, it may be more appropriate to evaluate the full time constant of the transient response (i.e., $\tau = R2 \cdot C$) to more accurately capture the system's dynamic characteristics.

4.2.5 *Effect of C-rate on Open Parallel Cell Voltage (V)*

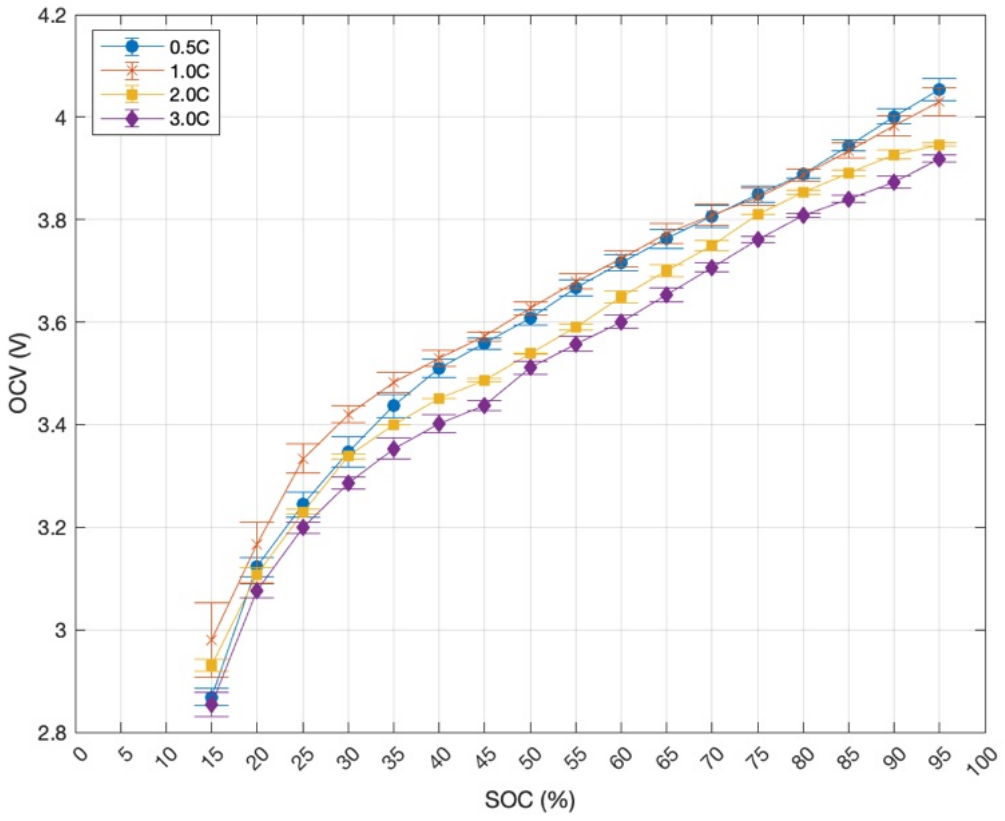


Figure 49: C-Rate Dependence of OCV (V) vs SOC (%) for a 6-Cell Parallel Stack of VTC6 Under GITT Discharge

Analyzing the average Open Circuit Voltage (OCV) vs. State of Charge (SOC) profiles reveals several notable patterns. First, the initial OCV at 95% SOC is similar for the 0.5C and 1C discharges, both starting around 4.05 V. The 2C and 3C discharges begin at a lower voltage, approximately 3.90 V. Throughout the early stages of discharge, the 0.5C and 1C profiles follow a nearly identical trend, with a slope of approximately 0.01 V/% SOC. While 2C and 3C also exhibit a similar slope, their profiles are offset downward by roughly 0.05 V and 0.1 V, respectively. Beyond 40% SOC, the discharge slope steepens for all C-rates, and the voltage profiles begin to converge. By approximately 15% SOC, all C-rates end up with terminal voltages between 2.85 V and 2.95 V. Measurement error

appears relatively consistent across all C-rates and SOC levels. For future work, it would be valuable to conduct a more detailed analysis at the SOC extremes. particularly at 100% and below 15% SOC. This could be achieved by applying short current pulses that capture all transient parameters without significantly discharging the battery.

4.2.6 *Effect of C-rate on internal parallel impedance R1 (Ω)*

The average internal impedance of the parallel configuration is strongly dependent on the C-rate. At lower C-rates, the internal impedance tends to spike at the end of the discharge, reaching peak values of approximately 0.012 Ω for 0.5C and 0.0083 Ω for 1C. Interestingly, at 3C, no such peak is observed at low SOC; instead, the impedance reaches its minimum in this region. Significant oscillations are observed above 30% SOC, much more pronounced than those seen in the single-cell tests (see Figure 40), which may be attributed to the smaller IR drops in the parallel configuration. Overall, the statistical error is greater in the parallel setup compared to the single cell, suggesting that voltage reading noise could be a key contributing factor. On average, the internal impedance of the parallel configuration ranges between 0.006 Ω and 0.002 Ω, which is approximately 6 to 17 times lower than that of the single-cell configuration.

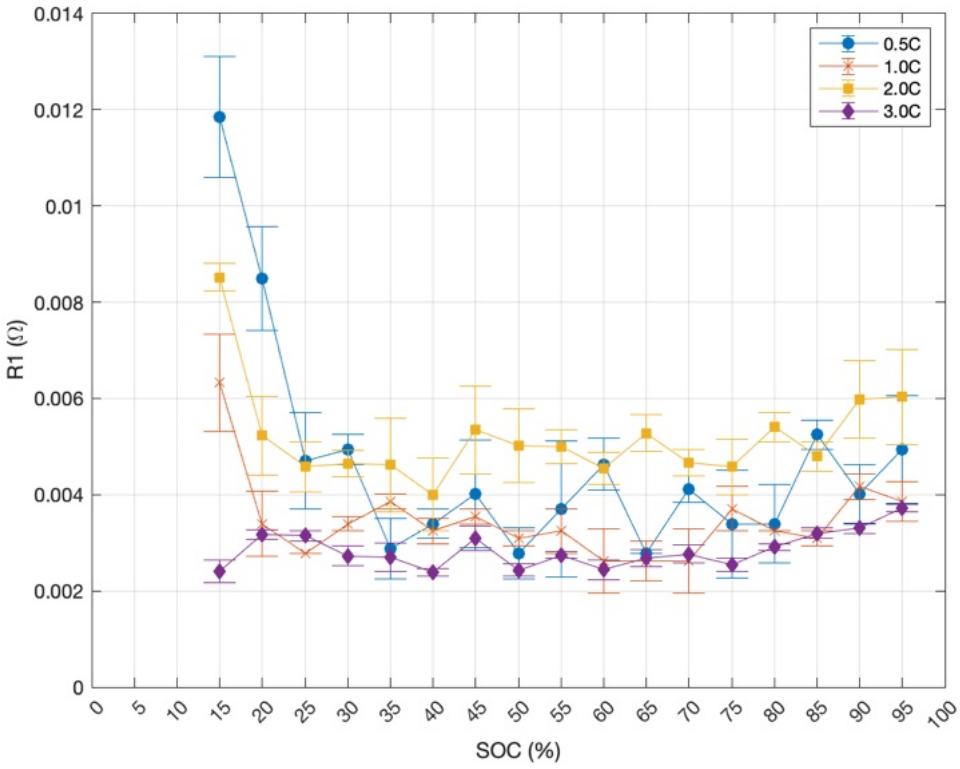


Figure 50: C-Rate Dependence of R1 (Ω) vs SOC (%) for a 6-Cell Parallel Stack of VTC6 Under GITT Discharge

4.2.7 *Effect of C-rate on parallel cell transient response*

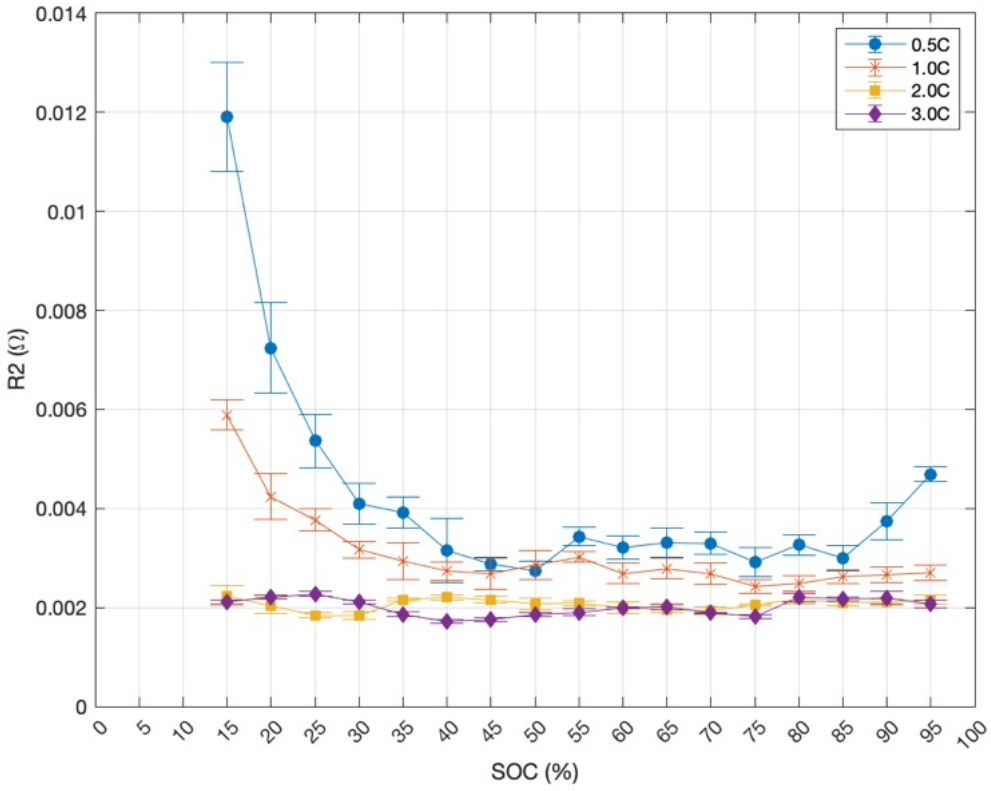


Figure 51: C-Rate Dependence of R2 (Ω) vs SOC (%) for a 6-Cell Parallel Stack of VTC6 Under GITT Discharge

The internal impedance R2 (Ω) of the parallel stack shows a noticeable dependence on discharge C-rate. At lower C-rates, a peak in R2 is observed toward the end of the discharge, reaching up to 0.012 Ω for 0.5C and 0.006 Ω for 1C. As the C-rate increases, R2 values tend to stabilize around 0.002 Ω from 2C onward. The error again stays relatively low consistent throughout the discharge. In contrast, the capacitance trends are less consistent across C-rates. Peaks occur at varying SOC values, typically between 30% and 65%, depending on the discharge rate (see Figure 52). These peaks generally approach 100,000 F and are often followed by a rapid decrease to values between 60,000 F and 30,000 F. These values are significantly higher, by a factor of 100 to 1000, compared to those observed for a single cell, which is far beyond the expected increase of around 6 times. This discrepancy suggests that further investigation is needed to fully validate the results. Given the oscillatory nature of the capacitance measurements, it may be more effective to evaluate the transient response using the overall time constant rather than relying solely on the individual R2–C components. Nevertheless, the extracted values still provide useful insights for modeling and simulation purposes.

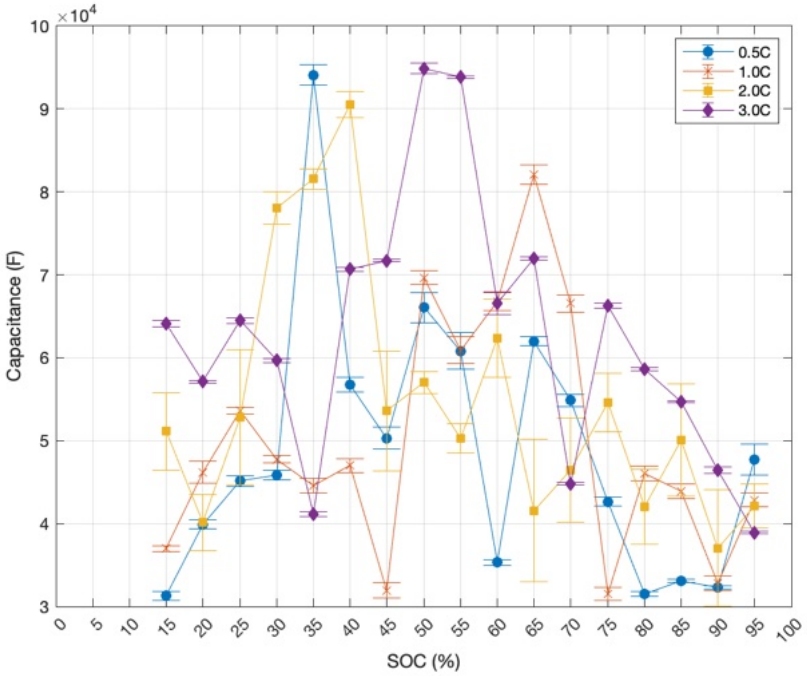


Figure 52: C-Rate Dependence of Capacitance (F) vs SOC (%) for a 6-Cell Parallel Stack of VTC6 Under GITT Discharge

4.3 *Scaling parallel and single cell models*

To further evaluate how battery cell models scale from a single cell to a parallel configuration, the results obtained from cycling the battery parallel were scaled down to the single-cell level. This allows for direct cell-to-cell comparison and validation against the manufacturer's datasheet, which only provides data at the single-cell level. The following assumptions were made in order to perform the downscaling:

First, all cells are assumed to be identical. While this may not hold in every case, it is a reasonable assumption given that all cells were purchased, stored, and tested under the same conditions, and the likelihood of significant factory defects is considered low. Based on this, the battery stack is modeled by its ECM: the combining its R1 and R2–C component. As established in Section 4.2.2, the equivalent resistance of a single cell is expected to be six times greater than that of the parallel configuration. Therefore, all resistance values (R1 and R2) from the parallel measurements are multiplied by 6 to estimate the single-cell equivalents. Conversely, since capacitance adds in parallel, the equivalent capacitance of a single cell is obtained by dividing the parallel capacitance by 6. Finally, the OCV remains unchanged when scaling, as all cells in the parallel configuration share the same voltage.

4.3.1 *Comparison of OCV vs SOC in Single-Cell and Scaled-Down Parallel configuration*

After scaling the parallel battery data down to the single-cell level, the first notable observation is that both the single cell and the scaled parallel configuration follow a similar OCV–SOC trend. At 0.5C (see Figure 53a), both profiles closely track the manufacturer's datasheet above 40% SOC, with the parallel configuration diverging slightly and dropping below the datasheet near the end of the discharge as the slope increases. For the higher C-rates (1C, 2C, and 3C), a small but noticeable offset appears at 95% SOC: the single-cell OCV begins approximately 0.03 V higher than the parallel at 1C, and up to 0.05 V higher at 2C and 3C.

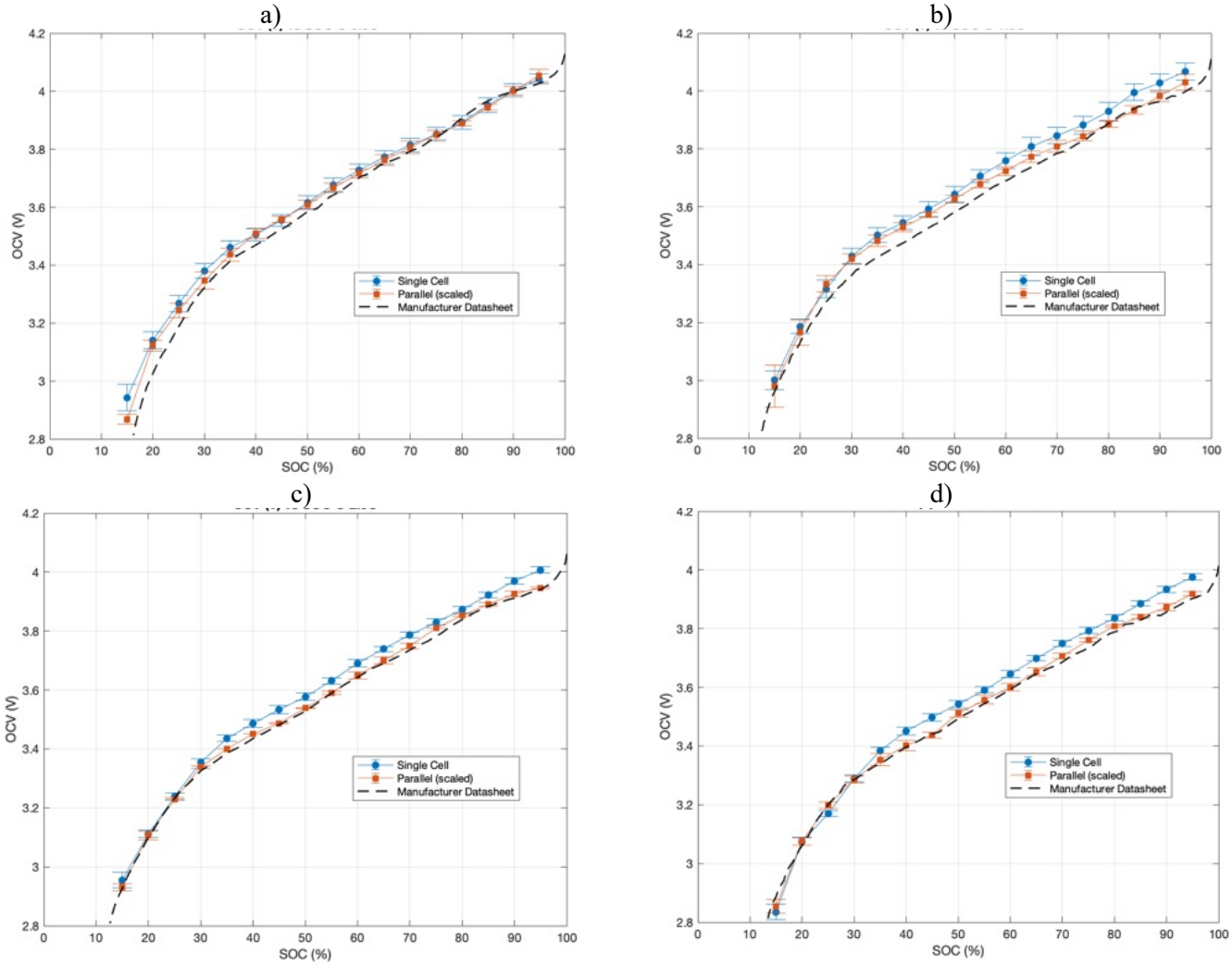


Figure 53: OCV (V) vs SOC (%) Comparison: Single Cell, Scaled Parallel Stack, and Manufacturer Datasheet Across Discharge C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

This offset gradually diminishes as the discharge progresses, with both profiles converging toward the datasheet values near the lower SOC range. Overall, the results suggest that the OCV–SOC relationship scales well from single cell to parallel configuration. While further validation is required to confirm this behavior at the module or pack level, there is currently no indication that the OCV–SOC profile would not scale consistently across system levels.

4.3.2 *Comparison of internal impedance (R1) in Single-Cell and Scaled-Down Parallel Models*

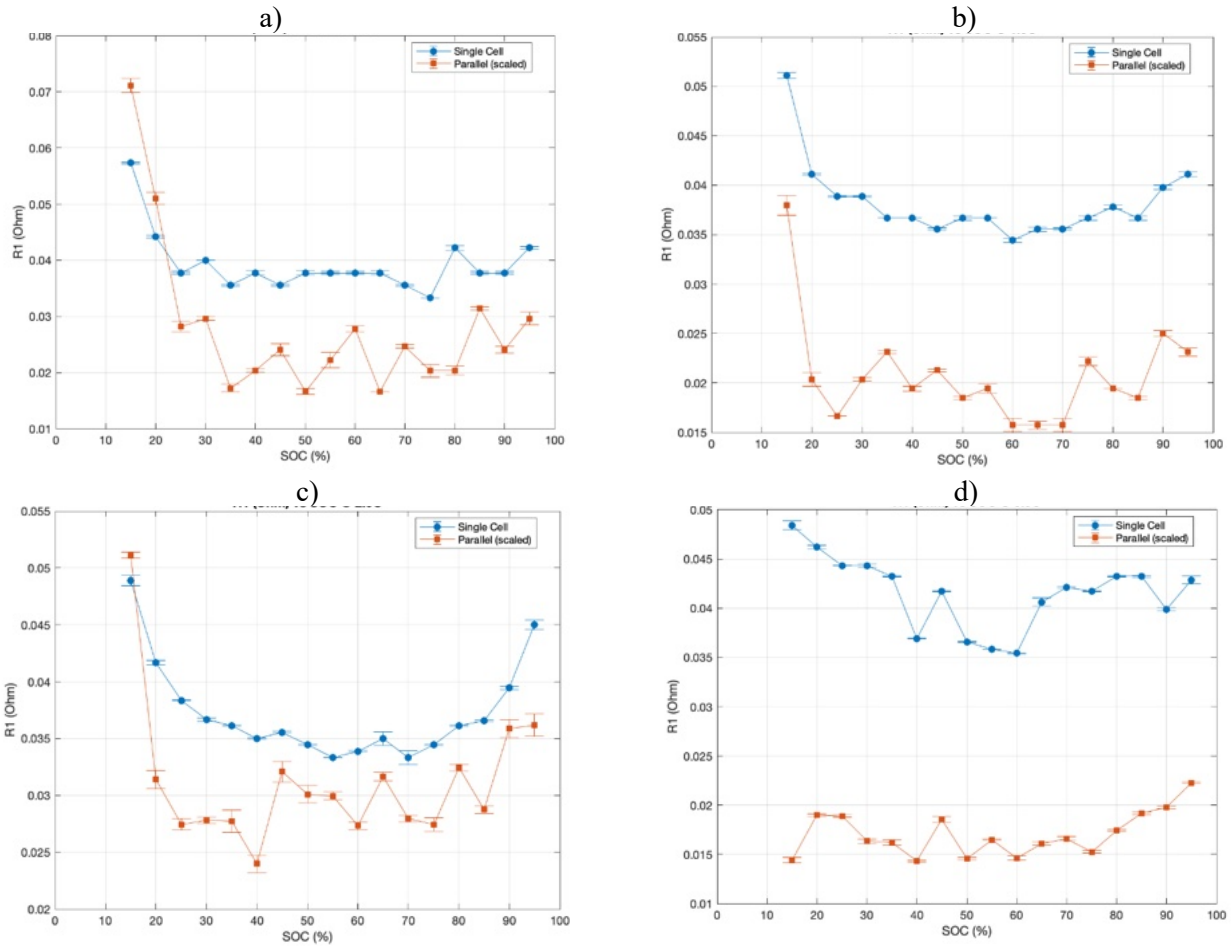


Figure 54: Internal Impedance R1 (Ω) vs SOC (%) Comparison: Single Cell, Scaled Parallel Stack, Across Discharge C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Contrary to the OCV–SOC profile, the internal impedance R1, does not scale as expected, at least not consistently across all C-rates. While there is a clear trend and some correspondence between the two scales (for example, Figure 54a shows similar peaks at 80–85% SOC and 15–25%, and Figures 54b and 54c show similar behavior at low SOC,

with both datasets showing a coinciding peak around 45% SOC in Figure 54d), the scaled-down internal impedance from the parallel configuration does not align well with the single-cell measurements. Several factors could be contributing to this discrepancy. First, the resolution of R1 measurements in the parallel configuration is inherently lower.

Scaling these values by a factor of six amplifies any measurement errors. Additionally, the voltage sensor for the single-cell setup was placed at the contactor rather than directly at the battery terminal. This introduces the potential for added resistance due to voltage drops in the connecting wires. Specifically, the wire used was an 8 cm length of 18 AWG, which has a resistance of 6.368 Ω per 1000 ft [35]. This results in an additional resistance of approximately 0.00180 Ω, comparable to the measured resistance values, especially in the parallel scale.

Furthermore, discrepancies in actual versus target current could have contributed to errors in the calculated resistance. This issue was particularly present in the 6-cell test bank, where fixed value shunt resistors regulated the current. In the worst-case scenario, this caused an offset between the set current and actual current of –2.87 A at maximum discharge (54 A). Internal resistance was calculated by dividing the voltage jump by the discharge current, under the assumption that the discharge current matched the setpoint. While this assumption held to the second decimal for the single-cell test bank, it was not valid for the 6-cell configuration. If the actual discharge current was, for example, 2.8 A lower than expected, the resulting IR voltage drop would be smaller than it would for 54A, leading to an underestimation of the calculated internal resistance. This could explain why the scaled internal impedance appears significantly lower than that of the single cell. One improvement to consider for future experiments would be the inclusion of an actual discharge current measurement using a Hall effect current sensor.

4.3.3 *Comparison of cell dynamic behavior in Single-Cell and Scaled-Down Parallel Models*

In a similar trend to R1, both R2 and the cell capacitance do not scale as expected. As shown in Figure 55a and 55b, R2 follows a somewhat similar trend at the end of the discharge, exhibiting a peak at 15% SOC, but it is far from being simply a scaled or offset version of the single-cell data. Notably, it lacks the distinct peaks and valleys observed at 45%, 80%, and 95% SOC in the single-cell case. The discrepancy becomes even more pronounced at higher C-rates, where the internal resistance is, on average, four to five times larger in the single cell than in the scaled parallel data. However, a more fundamental issue arises. Comparing the dynamic behavior of cells becomes challenging when both R2 and C are derived from the weights of an exponential fit. This complicates the interpretation of the transient dynamics. For future work, it would be beneficial to fix either the capacitance or the internal resistance R2 and instead model the transient response based on the time constant in combination with one of the two parameters.

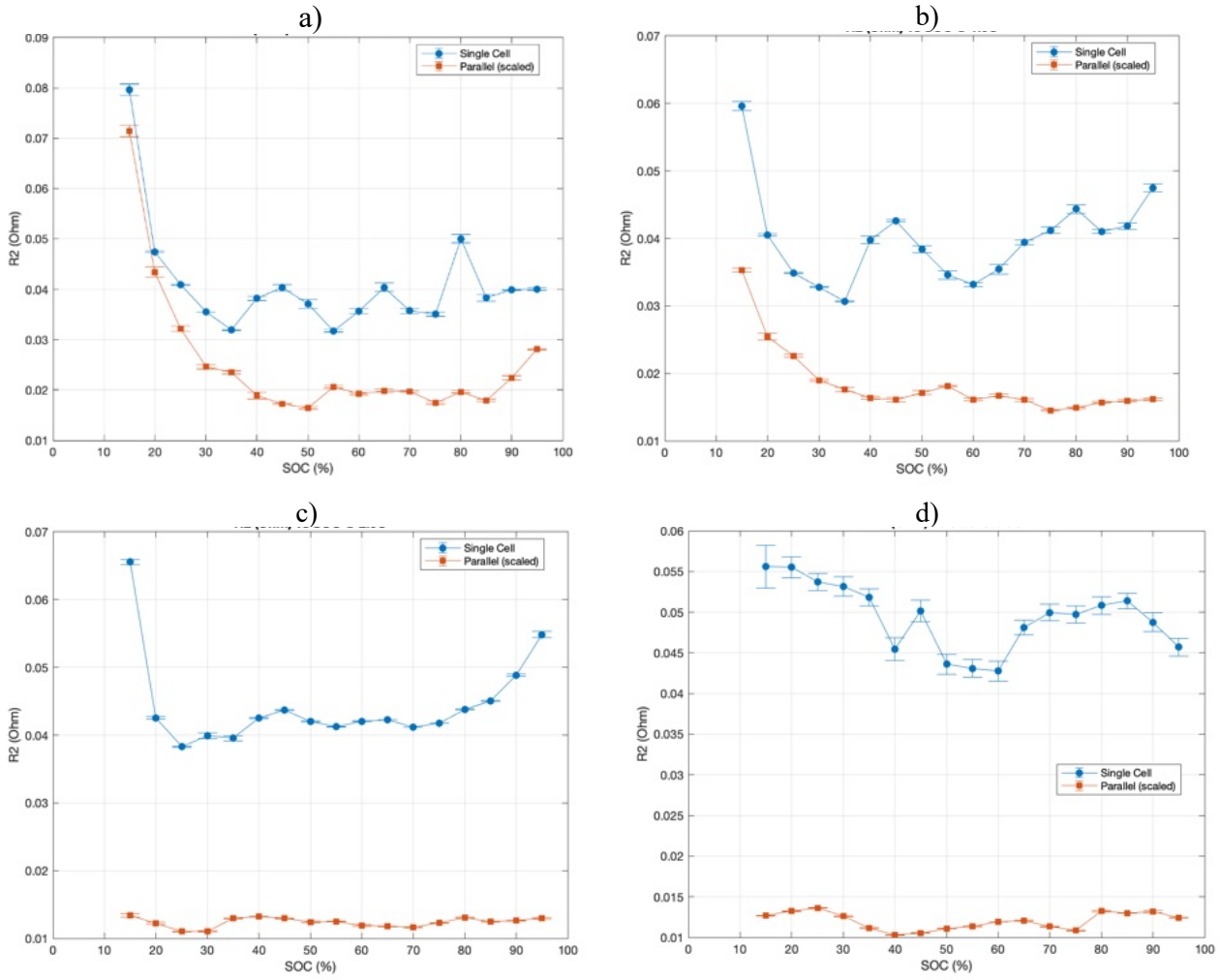


Figure 55: Internal Impedance R2 (Ω) vs SOC (%) Comparison: Single Cell, Scaled Parallel Stack Across Discharge C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

Figure 56 presents a comparison between the average capacitance of the single cell and the scaled-down average capacitance of the parallel battery stack. In the parallel configuration, capacitance peaks are observed within the 30%–80% SOC range depending on the C-rate, reaching up to approximately 18,000 F, while the highest peak for the single cell ranges between 100 F and 350 F. This results in a discrepancy of two to three orders of magnitude, with the scaled-down capacitance appearing 100–1000 times larger than that of the single cell. One key reason for this difference lies in how the weights for the exponential fitting are defined at each scale. The transient voltage response is modeled as:

$$v(t) = a * e^{-bt} + c$$

$$OCV\ (SOC) = c$$

$$R2(SOC) = a/I$$

$$C(SOC) = 1/(R2 * b)$$

Given that both R2 and C are derived parameters, discrepancies can easily arise depending on how a and b are fit at each scale. For more consistent comparison of the transient response across scales, it would be more insightful to analyze the raw fitting parameters a and b directly, rather than focusing solely on the derived values of R2 and C. However, it is true that the initial motivation for calculating R2 and C stemmed from their common use as dynamic input parameters in most ECM simulations.

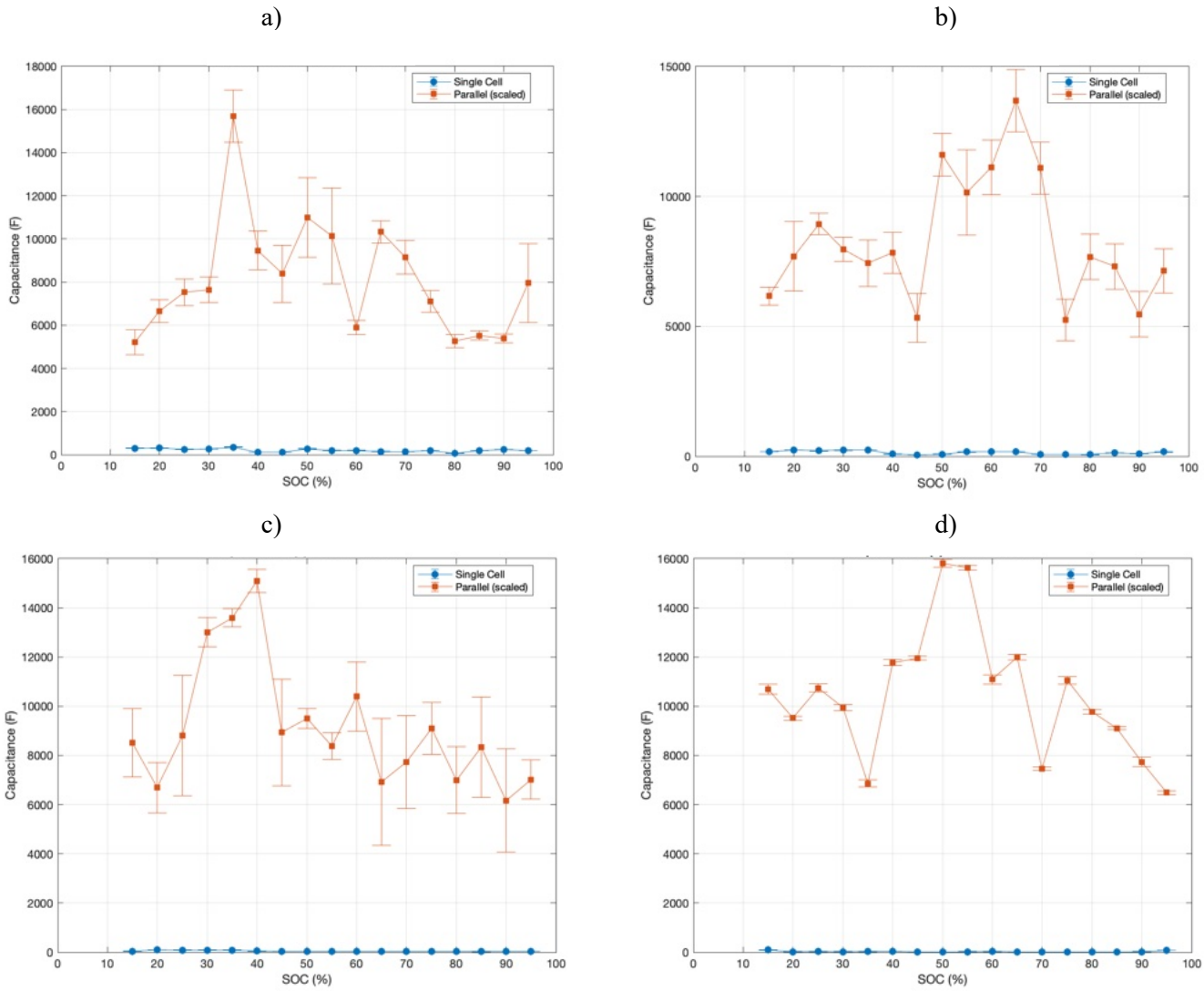


Figure 56: Internal Capacitance (F) vs SOC (%) Comparison: Single Cell, Scaled Parallel Stack Across Discharge C-Rates: a) 0.5C, b) 1C, c) 2C, d) 3C

5. Battery Modelling

Understanding how a battery cell scales from a single cell to a parallel stack is a crucial first step in developing any robust battery model. However, most EV battery packs do not stop at the parallel level, they are typically composed of several parallel groups connected in series to form modules, which are then assembled in series to create the full pack. Figure 57 below shows the battery modules used in the IFS-06 Formula Student race car. The pack consists of five modules, each containing 114 cells in a 19S6P configuration, resulting in a total pack configuration of 95S6P. This pack was chosen for modeling because it shares the same base parallel configuration as the one used in the six-cell test cycler.

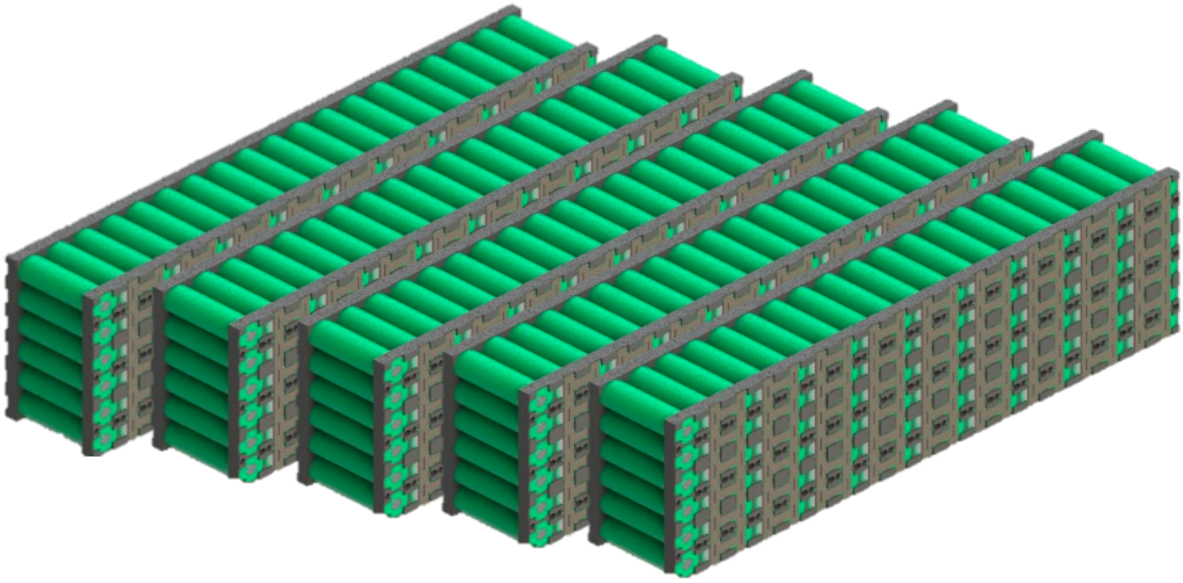


Figure 57: 18650 Sony VTC6 battery modules of the IFS-06 Formula Student Car

Using the data collected in Sections 4.1 and 4.2, a database was created in which OCV, R1, R2, and C were indexed by SOC and C-rate. This database was then imported into MATLAB Simscape and used to parameterize the base single-cell model for the SONY-MURATA INR US18650 VTC6. Additional information, such as battery mass and cell dimensions, was also included, resulting in the base model shown in Figure 58. For the simulation strategy, the MATLAB Simscape lumped cell model was chosen due to its fast simulation speed, ease of scaling to module and pack levels, and compatibility with other Simulink blocks, enabling more complex simulations to be performed within the same environment.

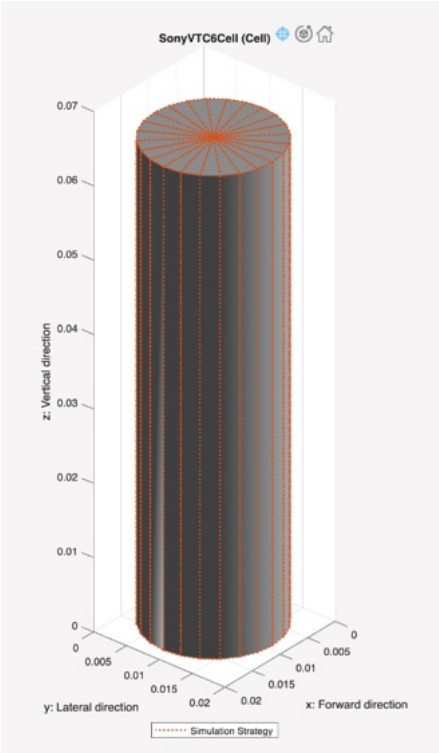


Figure 58: SONY-MURATA INR US18650 VTC6 MATLAB Simscape Cell Model

The base cell model was stacked to build the parallel assembly, as seen in Figure 59. One advantage of this simulation strategy was the ability to validate the parallel model against experimental data. After configuring the parallel assembly, it was exported as a Simulink library. The model was then subjected to a GITT load profile and discharged at a 1C rate.

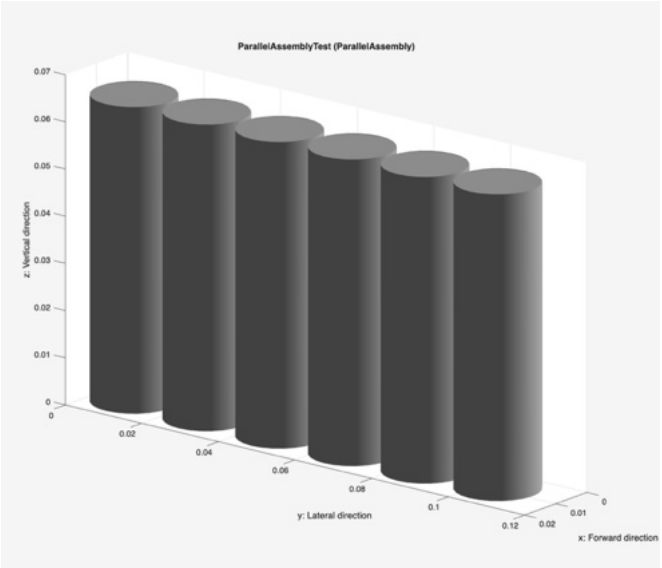


Figure 59: SONY VTC6 Parallel Assembly MATLAB Simscape Model

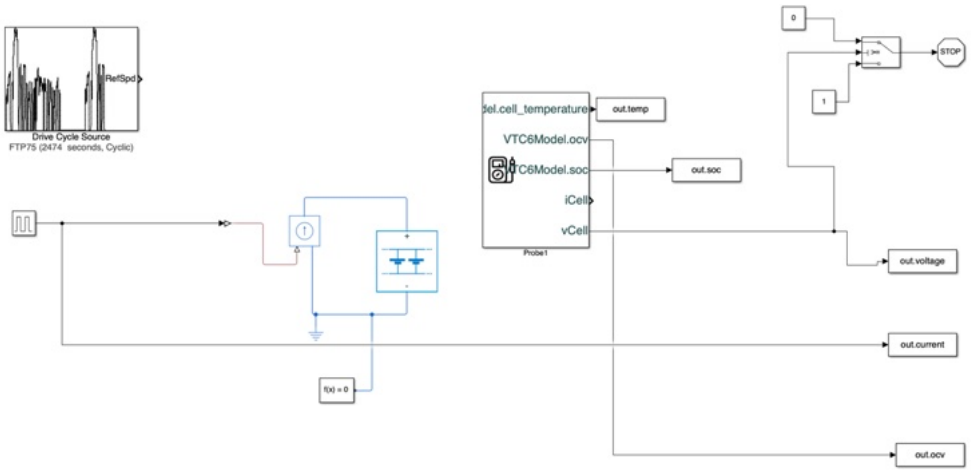


Figure 60: Parallel Assembly MATLAB Simulink Model

Figure 60 shows the parallel assembly integrated into a Simulink model, where a pulse modulator generates a 1C (18 A) GITT load profile, as illustrated in Figure 61a. The right-hand plot, Figure 61b, compares the simulated terminal voltage of the parallel stack with the measured voltage from the 1C run of the 6-cell parallel test bank. As seen in Figure 61b, the model generally follows the experimental voltage trend, though some discrepancies are evident, particularly at the start and end of the discharge. The simulated voltage begins at 4.0 V rather than the expected 4.2 V, due to the lack of proper mapping near 100% SOC, forcing the model to extrapolate. A similar issue appears at the end of the discharge, where the simulation plateaus prematurely instead of reaching 2.6 V. Additionally, while the model responds to current changes as expected, the transient dynamics do not closely follow the anticipated exponential behaviour, suggesting that further tuning of R2 and C is needed.

a) b)

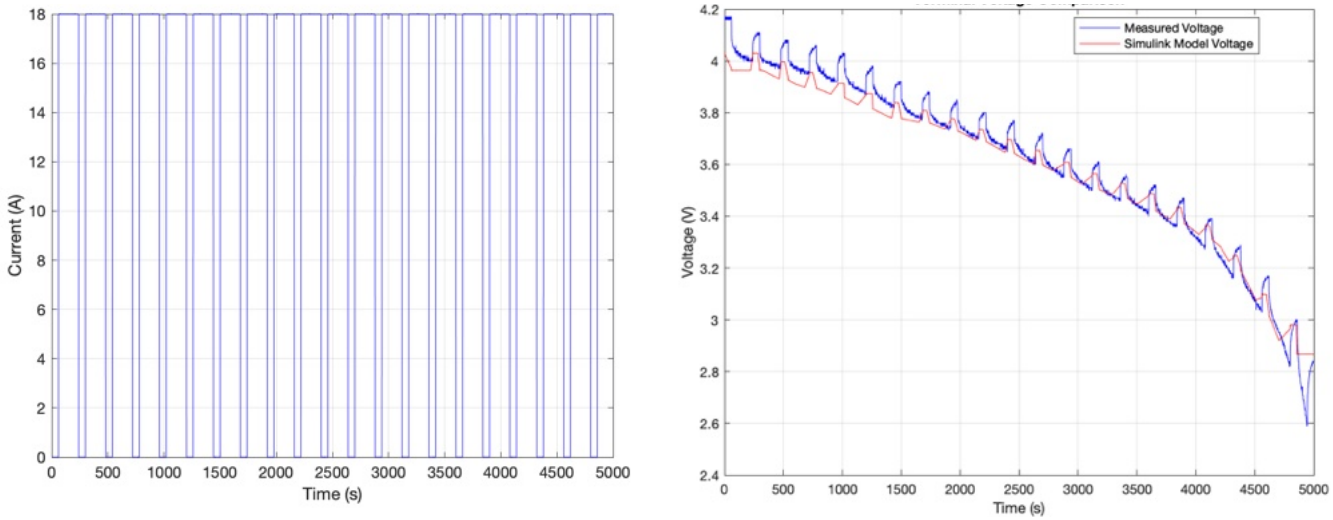


Figure 61: Parallel Cell Assembly 1C GITT Discharge in Simulink Simulation: a) Applied Current Profile, b) Terminal Voltage of Parallel Assembly

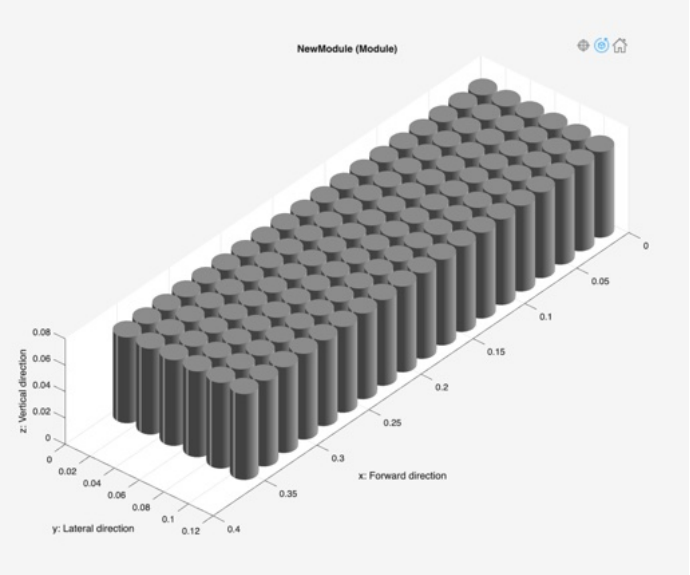


Figure 62: IFS-06 Formula Student Car battery modules Simscape assembly

After validating the parallel assembly against a real 1C test bank discharge, the next step was to build the module assembly by connecting 19 parallel groups in series, as shown in Figure 62. Once exported as a Simulink library, the module was discharged at 0.5C, 1C, 2C, and 3C. The corresponding discharge times before reaching the packs V_{min}, 47.5 V, were 6407 s, 3106 s, 1541 s, and 973 s, respectively. Interestingly, these discharge times were shorter than the theoretical durations because the voltage limit was set based on terminal voltage rather than OCV. As a result, the added ohmic drop caused the terminal voltage to hit the cutoff threshold earlier than expected.

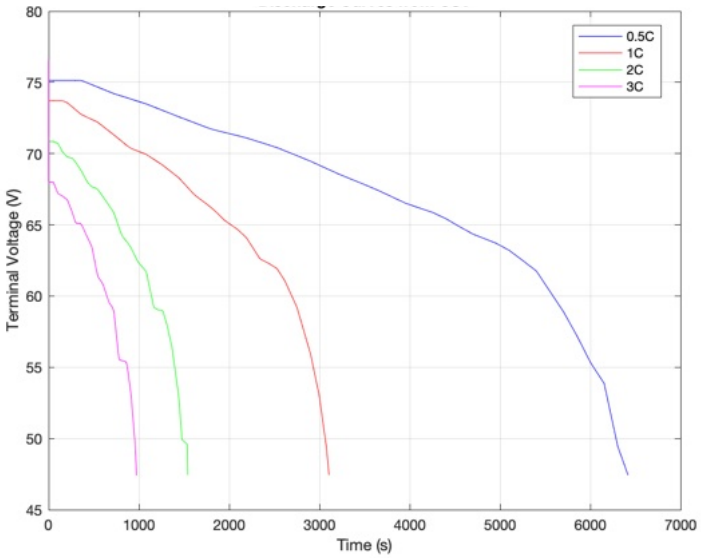


Figure 63: Simulink Simulation of Module Assembly Terminal Voltage (V) Under Different C-Rates: 0.5C, 1C, 2C, 3C

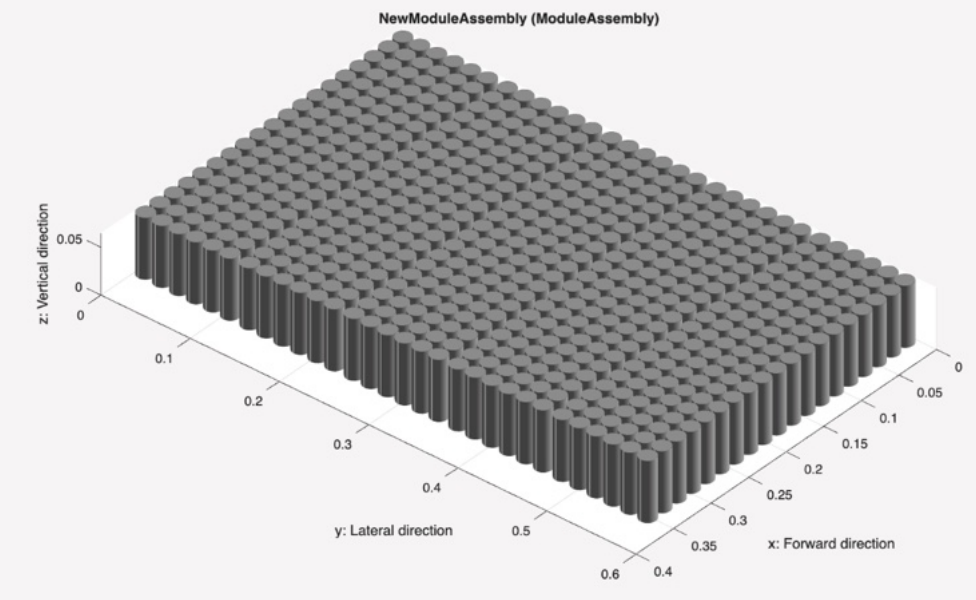


Figure 64: Simscape Assembly of the IFS-06 Formula Student Car Battery Pack

The final step in the scaling process was the pack level. Using the previously built module assembly, five modules were connected in series to construct the full battery pack, resulting in a 95S6P configuration, or what is the same, 570 Sony-Murata VTC6 cells in total. Figure 65 shows the Simulink library block representing the pack, which outputs real-time data, monitoring current, voltage, temperature, OCV, and SOC at the cell, module, and pack levels. The pack was subjected to a baseline stress test under four different discharge rates: 0.5C, 1C, 2C, and 3C. In each case, the pack was discharged from 100% SOC until it reached its V_{min} of 237.5 V (see Figure 66).

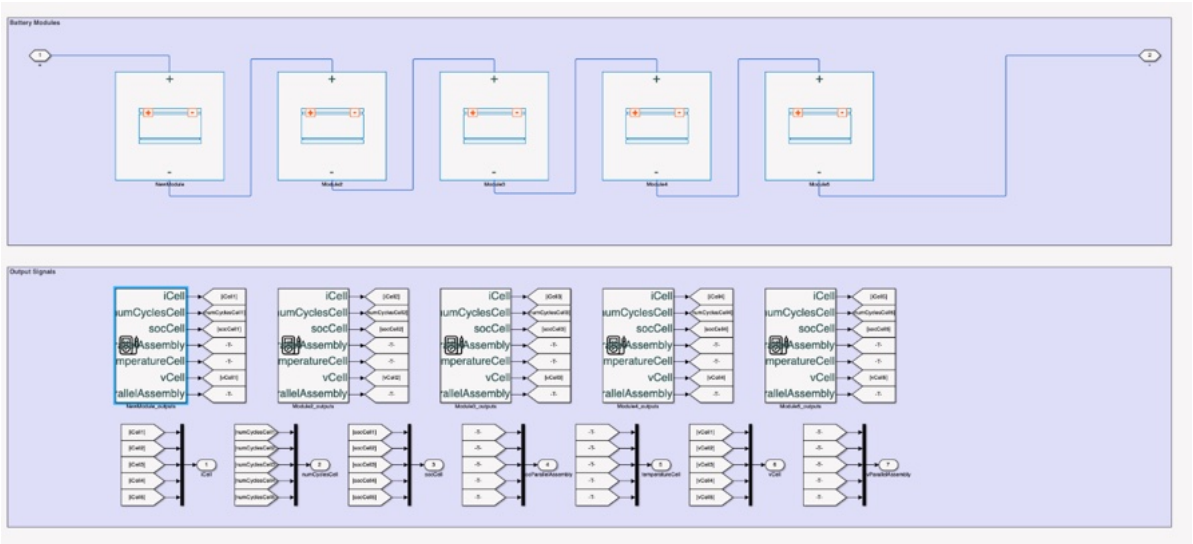


Figure 65: Pack Assembly Simulink Library Block

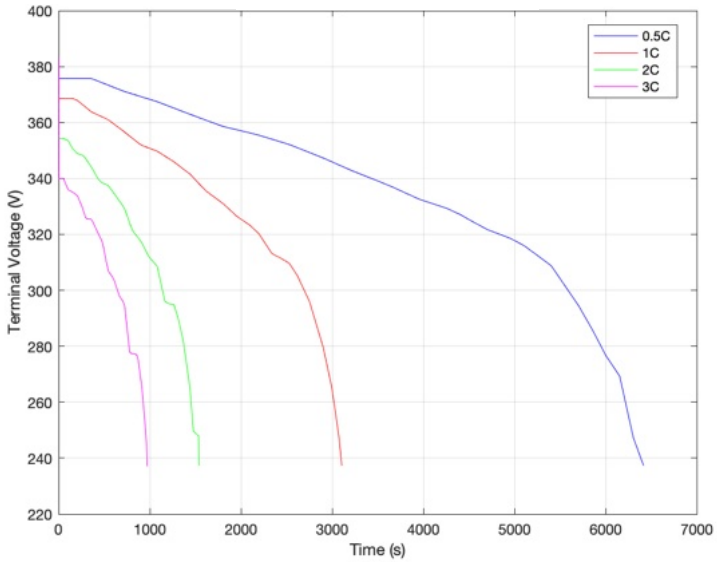


Figure 66: Simulink Simulation of Pack Assembly Terminal Voltage (V) Under Different C-Rates: 0.5C, 1C, 2C, 3C

In reality, although constant C-rates are useful for benchmarking and comparing different cells, they often do not reflect real-world operating conditions. To better simulate actual usage, the pack model was tested using MATLAB Simscape's integrated standardized drive cycle database. Specifically, the FTP-75 urban driving cycle was selected to represent city street conditions. Figure 67 shows the current drawn by the pack during the FTP-75 test. For the sake of simplicity, regen-braking was not included in this simulation. The FTP-75 drive lasts for around 30 minutes, capturing many realistic stop-and-go city traffic patterns, which were great to benchmark the battery pack under real-world conditions.

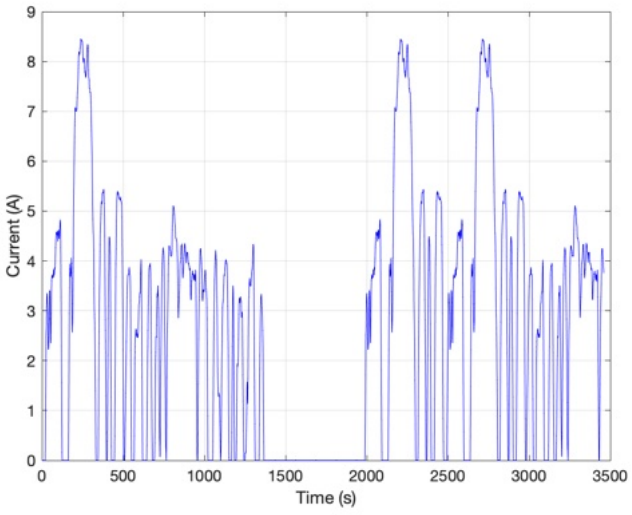


Figure 67: Pack current draw during various consecutive FTP-75 drive cycle

To further deplete the pack and obtain an extensive discharge characterization, multiple FTP-75 drive cycles were concatenated consecutively with rest periods in between. Figure 68 summarizes four key signals captured by the Simulink model during this extended test. Figure 68a) shows the terminal voltage, which starts at approximately 380 V and discharges down to around 270 V. Future updates to the model could extend the voltage profile beyond the current limits (beyond 95% and below 15% SOC), as the model currently struggles to extrapolate the OCV profile outside these ranges. In addition to electrochemical parameters, the model also simulates the thermal behavior of the module, reaching a peak temperature of 316.5 K (43.5 °C). It is important to note that this temperature was modeled using Simscape Battery's default thermal model without any active cooling solutions. Overall, the FTP-75 cycle serves as a realistic use case scenario for this type of model. Once saved as a Simulink library, the battery model can be integrated with virtually any other Simulink model, proving especially valuable when combined with powertrain and electric drive system simulations.

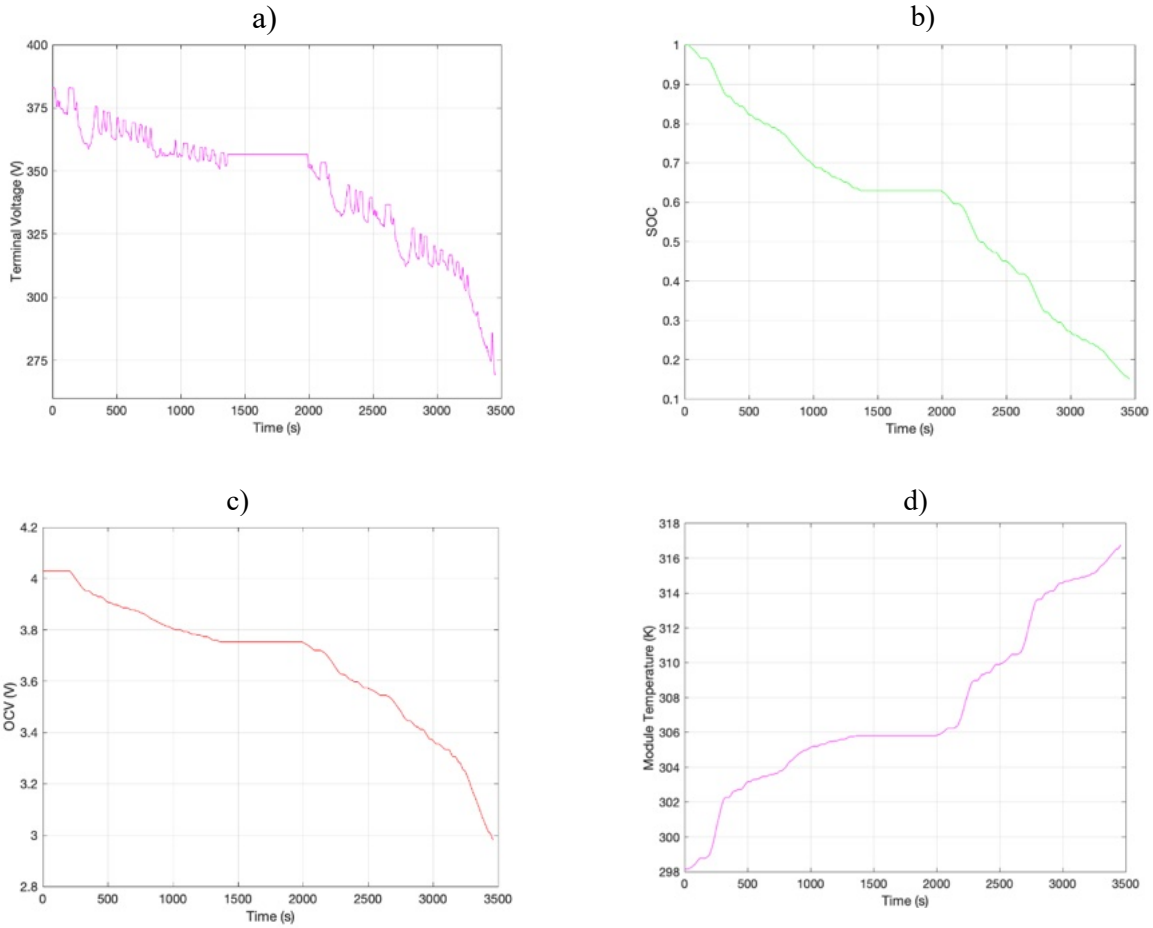


Figure 68: IFS-06 Formula Student Race Car Battery Pack FTP-75 Drive Cycle Simulink Simulation Results: a) Terminal Voltage (V) vs Time (s), b) SOC vs Time (s), c) OCV (V) vs Time (s), d) Module Temperature (K) vs Time (s)

6. Thermal Runaway Test

After completing all discharge tests for both the single cell and the parallel stack, a final round of destructive testing was carried out to further investigate the thermal runaway behavior of Sony-Murata VTC6 cells. Using the setup described in Section 3.2.4, five cells were charged to 20%, 60%, 80%, 90%, and 100% SOC, respectively. The objective was to understand how SOC influences the onset and severity of thermal runaway. The initial hypothesis was that cells at higher SOC would be more prone to thermal runaway. However, as shown in Figure 69, this was not entirely the case.

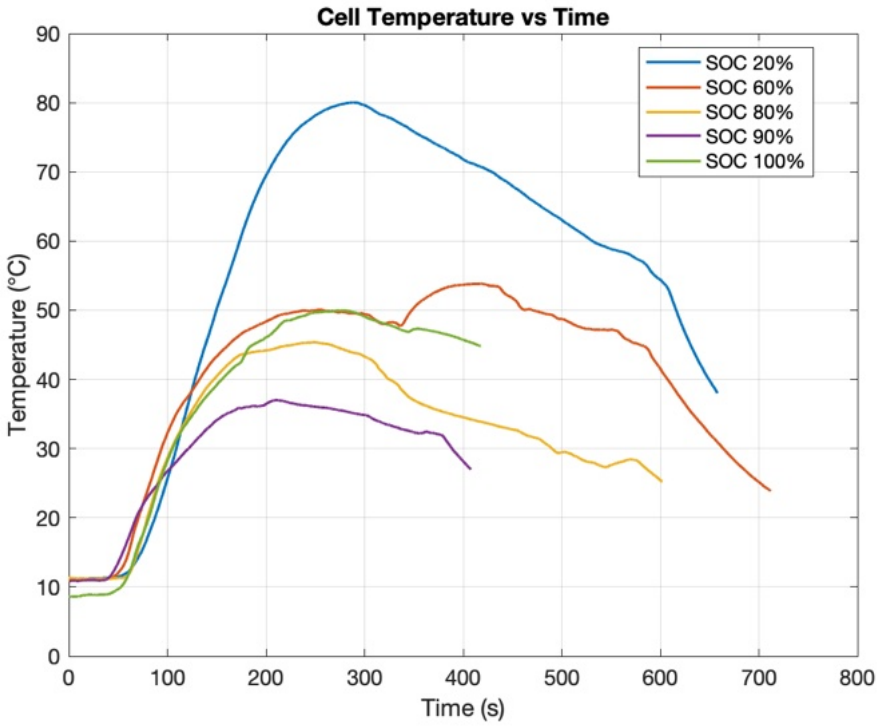


Figure 69: VTC6 Cell Temperature (Celsius) vs Time (s) after External Short-Circuit

Before analyzing the results, it is important to consider the boundary conditions of the experiment. The tests were conducted outdoors at an ambient temperature of 10 °C, with all cells stabilized to this environment prior to testing. As seen in Figure 69, none of the five cells entered thermal runaway. The highest temperature recorded was 80 °C, observed in the 20% SOC cell. All cells exhibited an initial temperature rise at roughly 0.4 °C/s, but after 80 seconds, the 60%, 80%, and 100% SOC cells showed a noticeable decline in their temperature growth rates. Interestingly, the 90% SOC cell was the first to exhibit this decline, with its rise stalling around 40 seconds into the test. In contrast, the 20% SOC cell continued to heat for over 200 seconds.

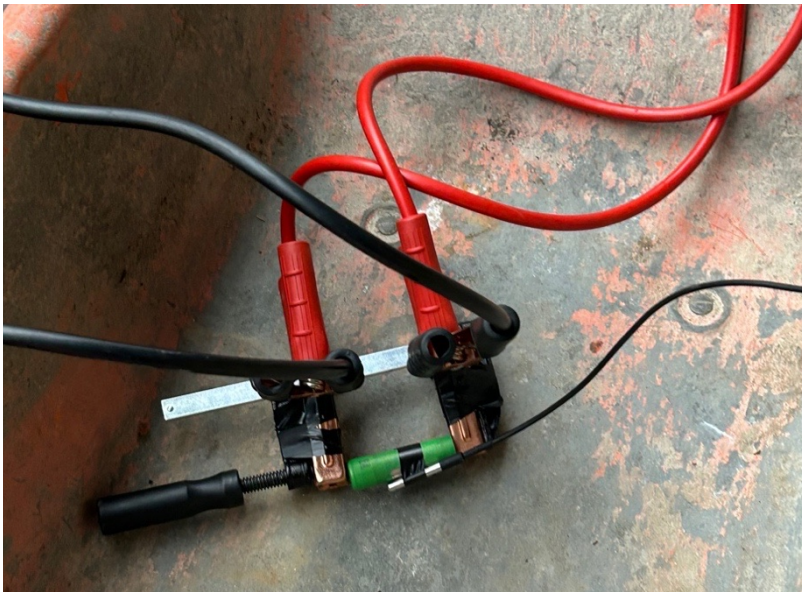


Figure 70: Sony VTC6 Cell undergoing ESC test @ 20% SOC

Initial SOC (%)	Venting Observed	Max Temperature (℃)
20%	No	80.00 ℃
60%	Yes	53.75 ℃
80%	Yes	45.31℃
90%	Yes	37.00 ℃
100%	Yes	49.81 ℃

Table 6: Venting and Max Temperature (℃) observed in each trial

One plausible explanation for this outcome lies in the venting mechanisms. As shown in Table 7, the 20% SOC cell did not vent—likely because its safety tab was not pierced—allowing internal pressure and heat to build up more than in the other cells. In contrast, all other cells exhibited clear signs of venting, which likely prevented further temperature escalation. Interestingly, the temperature profile of the 60% SOC cell shows a secondary thermal hump, suggesting a subsequent internal short circuit. However, this second event was likely insufficient to trigger thermal runaway on its own due to the limited energy remaining in the cell after the first short circuit. Additionally, the low ambient temperature (just 10 °C) may have inhibited the 20% SOC cell from reaching thermal runaway. It would be valuable to repeat this experiment under different ambient conditions and with an external short circuit method that bypasses the safety tabs to assess the consistency of these findings.

7. Sustainable Development Goals

The Sustainable Development Goals were drafted in 2015, by the United Nations as part of 2030 Agenda for Sustainable Development. They are broken down into 17 goals which aim to address the world's most pressing challenges, including climate change, energy access, resource efficiency, sustainable innovation and responsible consumption. This project directly supports three key SDGs: Goal 7: Affordable and Clean Energy, Goal 12: Responsible Consumption and Production, Goal 13: Climate Action

Goal 7 - Affordable and Clean Energy: One of the primary barriers to widespread adoption of clean energy technologies is the high cost of battery development and testing. This project contributes to SDG 7 by developing an affordable, accessible methodology for battery characterization. Through the use of low-cost components, such as Arduino controllers, modular resistor networks, and basic temperature sensors, this work enables advanced testing and modeling without the need for expensive commercial equipment. By lowering the entry barrier for battery research, the project promotes broader innovation in clean energy technologies, particularly in academic and small-scale industrial settings, accelerating the transition to sustainable energy systems.

Goal 12 - Responsible Consumption and Production: Battery manufacturing is resource-intensive, requiring rare earth materials and significant energy input. The environmental impact of battery production underscores the importance of maximizing battery lifespan. This project contributes to Goal 12 by enabling detailed monitoring and modeling of battery performance over time. By implementing SOC and SOH diagnostics, users can identify degradation trends early and adjust usage patterns accordingly, preventing overcharging, deep discharges, and thermal stress. This in-turn reduces electronic waste, supports circular economy principles, and leads to more responsible use of limited resources.

Goal 13 - Climate Action: Transportation is one of the largest contributors to global greenhouse gas emissions. Promoting the adoption of electric vehicles (EVs) is essential to achieving meaningful reductions in carbon emissions. By lowering the cost and complexity of battery testing, this project supports faster development and deployment of EV technologies. Furthermore, the integration of state-of-charge (SOC) and state-of-health (SOH) models allows for smarter battery management, extending battery lifespan and preventing failure modes that would otherwise lead to premature disposal. These improvements reduce both direct and indirect environmental impacts by directly contributing to reducing battery production and waste.

8. Conclusion

This study demonstrated a cost-effective and practical approach for battery characterization by developing two custom test benches: one for a single cell and another for a six-cell parallel configuration. The setups were capable of performing GITT discharges up to 3C—9 A for the single cell and up to 54 A for the parallel bank, matching performance levels typically limited to high-end commercial cyclers. Two current regulation strategies were explored: a MOSFET-based variable resistance offering high precision (±0.01 A) for lower currents, and a relay-controlled shunt resistor network, which enabled high-current cycling but introduced greater current deviation.

The test banks enabled extraction of key electrochemical parameters: OCV, R1, R2, and C across multiple C-rates (0.5C, 1C, 2C, 3C), allowing to develop equivalent circuit model for both single and parallel cell configurations. Analysis of OCV vs SOC revealed that higher C-rates consistently led to lower voltage profiles, especially at the beginning of discharge. Voltage curves across all C-rates began to converge below 30% SOC. R1 and R2 both exhibited U-shaped profiles for a single cell, with higher values at the start and end of discharge due to ion transport limitations. Capacitance values displayed complex trends with multiple peaks and valleys, particularly for 0.5C and 1C. These behaviors suggest underlying electrochemical dynamics that warrant further investigation, especially in relation to the transient response during deep discharge.

While OCV–SOC profiles scaled predictably from single cell to parallel configuration, the internal impedance and capacitance displayed greater variability. For instance, internal impedance in the parallel configuration was 17 times lower than in the single-cell case, not the expected 6x based on cell count alone. This discrepancy highlights both the complexity of scaling transient behavior and the limitations imposed by low-resolution voltage measurement. The use of a 10-bit Arduino ADC, with a quantization error of ±4.9 mV, constrained the ability to accurately capture the transient voltage profile (~50 mV) used to extract dynamic parameters such as R2 and C.

Nevertheless, using the higher-resolution single-cell parameters, an ECM database indexed by SOC and C-rate was developed and integrated into MATLAB Simscape. This enabled dynamic simulation of real-world load profiles and straightforward scaling to higher system levels, including modules and full battery packs. The selected modeling framework provided fast simulation times, and most importantly, a seamless integration with other Simulink power train components. The model was validated against a 95S6P battery pack from a Formula Student vehicle.

Finally, destructive short-circuit tests were conducted to investigate thermal runaway behavior across different SOC levels. None of the cells reached thermal runaway, with

the 20% SOC cell exhibiting the highest temperature (80 °C) and prolonged heating, likely due to the absence of venting. In contrast, all other cells vented, which helped limit thermal rise. Secondary thermal events, such as the hump observed in the 60% SOC cell, may indicate delayed internal short circuits. These results suggest that venting is a critical factor in mitigating thermal escalation.

In summary, this work presents a comprehensive, cost-effective, and practical approach for testing and characterizing ECMs for 18650 Li-ion cells using the Galvanostatic Intermittent Titration Technique, while also evaluating the scalability of single-cell models to parallel configurations. The insights and tools developed in this thesis can help lay the foundation for future early-stage research and development in both academic and small-scale industrial settings.

9. Future Work

Engineering a battery cycler capable of delivering discharge currents exceeding 50 A is a considerable challenge. Although the six-cell test bench can be regarded as a generally successful prototype, numerous lessons were learned throughout its development that would prompt several design improvements in a second iteration. While the relay-controlled shunt resistor network offered a simple and modular solution, its performance in current regulation was significantly inferior to the MOSFET-based approach. This was primarily due to the coarse step sizes and limited controllability of the shunt resistors. Future iterations should consider replacing the resistor array with a parallel bank of MOSFET-based variable loads to achieve finer current control. Additionally, incorporating Hall effect sensors and closing the regulation loop around current, rather than voltage, would enhance accuracy and dynamic stability.

It is also recommended to validate the ECM at higher system levels, including module and full pack configurations, to assess how simulation results scale relative to real EV hardware. Additionally, the extreme ends of the OCV–SOC curve could be more accurately characterized by conducting micro-discharge tests near 100% and below 15% SOC. Thermal modeling could also be expanded by validating ECM behavior under actual packaged cell conditions, which could help to quantify the temperature dependence of the internal impedance and capacitance. Finally, it may be valuable to repeat the thermal runaway experiments under nominal ambient temperatures (25 °C–40 °C) that better reflect typical operating conditions. Additionally, exploring alternative short-circuit methods, such as nail penetration tests that directly induce internal shorts, could provide deeper insight into failure thresholds and runaway mechanisms.

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Annexes

Annex 1: C++ Arduino Relay Control Script and Datalogger

```
#include <arduino.h>
#include "class_temp0.h"

// Define pin numbers for relays and analog inputs
#define REL1 53
#define REL2 51
#define REL3 49
#define REL4 47
#define REL5 45
#define REL6 43
#define REL7 41
#define REL8 39
#define REL9 37
#define REL10 35
#define REL11 33
#define REL12 7
#define V A0
#define A A1

// Define object for temperature readings
Temperatures temperaturas(0, 0);

void controlRelays(float voltage);

void setup() {
  // Set relay pins as outputs
  pinMode(REL1, OUTPUT);
  pinMode(REL2, OUTPUT);
```

```
  pinMode(REL3, OUTPUT);
  pinMode(REL4, OUTPUT);
  pinMode(REL5, OUTPUT);
  pinMode(REL6, OUTPUT);
  pinMode(REL7, OUTPUT);
  pinMode(REL8, OUTPUT);
  pinMode(REL9, OUTPUT);
  pinMode(REL10, OUTPUT);
  pinMode(REL11, OUTPUT);
  pinMode(REL12, OUTPUT);

  // Initialize serial communication
  Serial.begin(115200);
}

void loop() {
  unsigned long currentTime = millis();
  static unsigned long relay12StartTime = 0;
  static bool relay12State = LOW;

  if (relay12State == HIGH && currentTime - relay12StartTime >= 360000) {
    relay12State = LOW;  // Turn off relay 12 after 180 seconds
    digitalWrite(REL12, relay12State);
    relay12StartTime = currentTime;
  } else if (relay12State == LOW && currentTime - relay12StartTime >= 60000) {
    relay12State = HIGH; // Turn on relay 12 after 60 seconds of being off
    digitalWrite(REL12, relay12State);
    relay12StartTime = currentTime;
  }

  // Record data every 1 second
  static unsigned long lastDataRecordTime = 0;
  if (currentTime - lastDataRecordTime >= 1000) {
```

```
//tdelta=currentTime-lastDataRecordTime; (check loop speed)
lastDataRecordTime = currentTime;
int REL_1=LOW;
int REL_2=LOW;
int REL_3=LOW;
int REL_4=LOW;
int REL_5=LOW;
int REL_6=LOW;
int REL_7=LOW;
int REL_8=LOW;
int REL_9=LOW;
int REL_10=LOW;
int REL_11=LOW;
float vr;

int tension = analogRead(V);
//int corriente = analogRead(A);
if(relay12State == HIGH){
  vr = tension * (4.912 / 1023.0);
  //float cr = ((corriente * (5.0 / 1023.0)) - 2.4) / 2.4 * 150 - 60;
}

if(relay12State == LOW){
  vr = tension * (4.956 / 1023.0);
  //float cr = ((corriente * (5.0 / 1023.0)) - 2.4) / 2.4 * 150 - 60;
}

Serial.print(lastDataRecordTime);
Serial.print(",");
temperaturas.Measure_Temp();
Serial.print(vr);
Serial.print(",");
//Serial.print(cr);
```

```
Serial.println(";");


if(vr >= 4.05){
  REL_1=HIGH;
  REL_2=HIGH;
}
else if(vr >= 3.9){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
}
else if(vr >= 3.75){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
}
else if(vr >= 3.6){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
}
else if(vr >= 3.45){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
}
else if(vr >= 3.7){
```

```
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
  REL_7=HIGH;
}
else if(vr >= 3.15){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
  REL_7=HIGH;
  REL_8=HIGH;
}
else if(vr >= 3){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
  REL_7=HIGH;
  REL_8=HIGH;
  REL_9=HIGH;
}
else if(vr >= 2.85){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
```

```
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
  REL_7=HIGH;
  REL_8=HIGH;
  REL_9=HIGH;
  REL_10=HIGH;
}
else if(vr >= 2.5){
  REL_1=HIGH;
  REL_2=HIGH;
  REL_3=HIGH;
  REL_4=HIGH;
  REL_5=HIGH;
  REL_6=HIGH;
  REL_7=HIGH;
  REL_8=HIGH;
  REL_9=HIGH;
  REL_10=HIGH;
  REL_11=HIGH;
}

digitalWrite(REL1,REL_1);
digitalWrite(REL2,REL_2);
digitalWrite(REL3,REL_3);
digitalWrite(REL4,REL_4);
digitalWrite(REL5,REL_5);
digitalWrite(REL6,REL_6);
digitalWrite(REL6,REL_6);
digitalWrite(REL7,REL_7);
digitalWrite(REL8,REL_8);
digitalWrite(REL9,REL_9);
digitalWrite(REL10,REL_10);
```

```
  digitalWrite(REL11,REL_11);

  if(vr <2.5){
    relay12State = LOW;
    relay12StartTime=currentTime + 60000;
    digitalWrite(REL12, relay12State);
  }
 }
}
```

Annex 2: Source Code Matlab Simscape Parallel Model

```
component ParallelAssemblyTest
    % ParallelAssemblyTest:2
    % Parallel Assembly Block
    %    Model resolution: Lumped
    %    Number of cells: 6

    %    MATLAB version: 23.2
    %    Simscape Battery version: 23.2
    %    Simscape code generated on: 28-Jun-2025 11:57:20

    parameters
        SOC_vecCell = {[0,0.05,0.1,0.15, 0.2, 0.25, 0.3, 0.35, 0.4,
0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.75, 0.8, 0.85, 0.9, 0.95],'1'}; %
Vector of state-of-charge values, SOC
        V0_vecCell = {[2.98006876, 3.16528340, 3.33319366, 3.42020010,
3.48298779, 3.52947170, 3.57194770, 3.62672152, 3.67898049,
3.72309359, 3.77297140, 3.80909767, 3.84422792, 3.88677546,
3.93482891, 3.98341658, 4.02986491],'V'}; % Open-circuit voltage,
V0(SOC)
        V_rangeCell = {[0, inf],'V'}; % Terminal voltage operating
range [Min Max]
        R0_vecCell = {[0.03796296, 0.02037036, 0.01666668, 0.02037036,
0.02314812, 0.01944444, 0.02129628, 0.01851852, 0.01944444,
0.01574076, 0.01574076, 0.01574076, 0.02222220, 0.01944444,
0.01851852, 0.02500002, 0.02314812],'Ohm'}; % Terminal resistance,
R0(SOC)
        AHCell = {18,'A*hr'}; % Cell capacity, AH
        extrapolation_optionCell =
{simscape.enum.extrapolation.nearest,'1'}; % Extrapolation method for
all tables
        R1_vecCell = {[0.0588390, 0.0423960, 0.0376748, 0.0316261,
0.0393740, 0.0273067, 0.0268119, 0.0285320, 0.0301964, 0.0268959,
0.0278493, 0.0268247, 0.0241976, 0.0248029, 0.0261756, 0.0265589,
0.0269442],'Ohm'}; % First polarization resistance, R1(SOC)
        tau1_vecCell =
{[42.8395,32.8185,43.8544,46.0517,31.5415,66.5234,82.0794,66.7582,60.8
944,69.6491,31.939,46.9865,44.5797,47.7684,53.6131,46.1966,36.9873],'s
'}; % First time constant, tau1(SOC)
        thermal_massCell = {100,'J/K'}; % Thermal mass
    end

    parameters(ExternalAccess=none)
        P = 6; % Batteries in Parallel
    end

    nodes
        p = foundation.electrical.electrical; % +
        n = foundation.electrical.electrical; % -
    end

    variables
```

```
        iCell = {0,'A'}; % Cell current (positive in)
        vCell = {0,'V'}; % Cell terminal voltage
        socCell = {value={1,'1'},priority=priority.high}; % Cell state
of charge
        numCyclesCell = {value={0,'1'},priority=priority.high}; % Cell
discharge cycles
        temperatureCell = {value={298.15,'K'},priority=priority.high};
% Cell temperature
        vParallelAssembly = {value={0,'V'},priority=priority.none}; %
Parallel Assembly Voltage
        socParallelAssembly = {value={1,'1'},priority=priority.none};
% Parallel Assembly state of charge
    end

    intermediates
        power_dissipated = SonyMurataVTC618650.power_dissipated*(P-1);
% Power dissipated by P-1 cells
    end

    equations
        assert(length(iCell) == 1);
        assert(length(vCell) == 1);
        assert(length(socCell) == 1);
        assert(length(numCyclesCell) == 1);
        assert(length(temperatureCell) == 1);
        assert(length(vParallelAssembly) == 1);
        assert(length(socParallelAssembly) == 1);
        vParallelAssembly == SonyMurataVTC618650(1).p.v -
SonyMurataVTC618650(1).n.v;
        socParallelAssembly == SonyMurataVTC618650.stateOfCharge;
        SonyMurataVTC618650.i == iCell;
        SonyMurataVTC618650.v == vCell;
        SonyMurataVTC618650.stateOfCharge == socCell;
        SonyMurataVTC618650.num_cycles == numCyclesCell;
        SonyMurataVTC618650.cell_temperature == temperatureCell;
    end

    components(ExternalAccess=observe)
        SonyMurataVTC618650 = batteryecm.table_battery(SOC_vec =
SOC_vecCell,...
            V0_vec = V0_vecCell,V_range = V_rangeCell,R0_vec =
R0_vecCell,AH = AHCell,...
            extrapolation_option = extrapolation_optionCell,R1_vec =
R1_vecCell,...
            tau1_vec = tau1_vecCell,thermal_mass =
thermal_massCell,...
            T_dependence =
simscape.enum.tablebattery.temperature_dependence.no,...
            prm_age_OCV =
simscape.enum.tablebattery.prm_age_OCV.OCV,...
            prm_age_capacity =
simscape.enum.tablebattery.prm_age.disabled,...
            prm_age_modeling =
simscape.enum.tablebattery.prm_age_modeling.equation,...
```

```
            prm_age_resistance =
simscape.enum.tablebattery.prm_age.disabled,...
            prm_dir =
simscape.enum.tablebattery.prm_dir.noCurrentDirectionality,prm_dyn =
simscape.enum.tablebattery.prm_dyn.rc1,...
            prm_fade =
simscape.enum.tablebattery.prm_fade.disabled,...
            prm_leak =
simscape.enum.tablebattery.prm_leak.disabled,...
            thermal_port =
simscape.enum.thermaleffects.model,i.priority =
priority.none,v.priority = priority.none,...
            stateOfCharge.priority = priority.none,num_cycles.priority
= priority.none,...
            cell_temperature.priority = priority.none);
    end

    components(Access=private)
        PositiveAdapter =
BatteriesLumpingAdapters.ElectricalLumpingAdapter(CellsInParallel =
P);
        NegativeAdapter =
BatteriesLumpingAdapters.ElectricalLumpingAdapter(CellsInParallel =
P);
    end

    connections
        connect(n,NegativeAdapter.LumpedNode);
        connect(NegativeAdapter.CellNode,SonyMurataVTC618650.n);
        connect(p,PositiveAdapter.LumpedNode);
        connect(PositiveAdapter.CellNode,SonyMurataVTC618650.p);
    end

    annotations
        [p] : Side=top;
        [n] : Side=bottom;
        UILayout =
[UIGroup("Main",SOC_vecCell,V0_vecCell,V_rangeCell,R0_vecCell,AHCell,e
xtrapolation_optionCell),...

UIGroup("Dynamics",R1_vecCell,tau1_vecCell),UIGroup("Thermal",thermal_
massCell)];
        Icon = 'parallelAssembly.svg';
    end
end
```